XR806 IC

用户手册

版本号：1.1

发布时间：2022-04-27

版本历史

版本	日期	责任人	版本描述
1.1	2022-04-27	AWA 1091	修改部分描述信息。
1.0	2021-08-25	AWA 1091	创建文档。

目录

版本历史 i
目录 ii
图片目录 xvi
表格目录 xvii
1 前言 18
1.1 文档简介 18
1.2 目标读者 18
1.3 适用范围 18
1.4 文档约定 18
1.4.1 标志说明 18
1.4.2 地址与数据描述方法约定 18
1.4.3 数值单位约定 19
2 系统和存储 20
2.1 XR806 应用子系统 20
2.1.1 概述 20
2.1.2 功能描述 21
2.1.2.1 系统框图 21
2.1.2.2 关键特性 22
2.1.2.3 NVIC 寄存器列表 24
2.1.3 中断寄存器描述 25
2.2 系统控制模块（SYSCTRL） 27
2.2.1 概述 27
2.2.2 SYSCTRL 寄存器列表 27
2.2.3 SYSCTRL 寄存器描述 27
2.2.3.1 SIP_FLASH_TEST_MAP_REG 27
2.2.3.2 PS_CTL_REG 28
2.2.3.3 PS_CNT_REG 29
2.2.3.4 FLASH_PSARM_PIN_MAP_REG 29
2.2.3.5 GENERAL_DBG0_REG 29
2.2.3.6 GENERAL_DBG1_REG 30
2.3 存储空间映射（Memory Mapping） 31
2.4 存储控制器（Memory Controller） 32
2.4.1 概述 32

2.4.2 编程指引 32
2.4.3 Memory Controller 寄存器列表 33
2.4.4 Memory Controller 寄存器描述 35
2.4.4.1 MEM_COM_CFG_REG 35
2.4.4.2 SQPI_COM_CFG_REG 37
2.4.4.3 CACHE_CFG_REG 37
2.4.4.4 MEM_AC_CFG_REG 38
2.4.4.5 FLASH_C_READ_CFG_REG 38
2.4.4.6 FLASH_C_WRITE_CFG_REG 40
2.4.4.7 FLASH_C_RD_DUMMY_H_REG 42
2.4.4.8 FLASH_C_RD_DUMMY_L_REG 42
2.4.4.9 FLASH_C_WR_DUMMY_H_REG 42
2.4.4.10 FLASH_C_WR_DUMMY_L_REG 42
2.4.4.11 FLASH_C_IO_SWIT_TIME_REG 42
2.4.4.12 S_RW_CFG_REG 42
2.4.4.13 S_ADDR_CFG_REG 44
2.4.4.14 S_DUMMY_H_REG 44
2.4.4.15 S_DUMMY_L_REG 44
2.4.4.16 S_IO_SWIT_TIME_REG 44
2.4.4.17 S_WR_NUM_REG 44
2.4.4.18 S_RD_NUM_REG 45
2.4.4.19 START_SEND_REG_REG 45
2.4.4.20 FIFO_TRIG_LEV_REG 46
2.4.4.21 FIFO_STA_REG_REG 46
2.4.4.22 INT_EN_REG_REG 47
2.4.4.23 INT_STA_REG_REG 48
2.4.4.24 FLASH_MOD_EXE_IND_REG 49
2.4.4.25 START_ADDR0_REG 50
2.4.4.26 END_ADDR0_REG 50
2.4.4.27 BIAS_ADDR0_REG 50
2.4.4.28 START_ADDR1_REG 50
2.4.4.29 END_ADDR1_REG 51
2.4.4.30 BIAS_ADDR1_REG 51
2.4.4.31 START_ADDR2_REG 51
2.4.4.32 END_ADDR2_REG 51
2.4.4.33 BIAS_ADDR2_REG 52
2.4.4.34 START_ADDR3_REG 52
2.4.4.35 END_ADDR3_REG 52
2.4.4.36 BIAS_ADDR3_REG 52
2.4.4.37 START_ADDR4_REG 53
2.4.4.38 END_ADDR4_REG 53
2.4.4.39 BIAS_ADDR4_REG 53
2.4.4.40 START_ADDR5_REG 53

2.4.4.41 END_ADDR5_REG....54
2.4.4.42 BIAS_ADDR5_REG....54
2.4.4.43 S_WDATA_REG....54
2.4.4.44 S_RDATA_REG....54
2.4.4.45 PSRAM_ COM_CFG_REG....54
2.4.4.46 PSRAM_CTRL_COM_CFG_REG....55
2.4.4.47 PSRAM_CACHE_CFG_REG....55
2.4.4.48 PSRAM_C_READ_CFG_REG....55
2.4.4.49 PSRAM_C_WRITE_CFG_REG....57
2.4.4.50 PSRAM_C_RD_DUMMY_H_REG....58
2.4.4.51 PSRAM_C_RD_DUMMY_L_REG....59
2.4.4.52 PSRAM_C_WR_DUMMY_H_REG....59
2.4.4.53 PSRAM_C_WR_DUMMY_L_REG....59
2.4.4.54 PSRAM_C_IO_SWIT_TIME_REG....59
2.4.4.55 PSRAM_FORCE_CFG_REG....59
2.4.4.56 PSRAM_COM_CFG_REG....60
3 时钟和复位....61
3.1 全局电源、复位、时钟管理（GPRCM）....61
3.1.1 概述....61
3.1.2 GPRCM 寄存器列表....61
3.1.3 GPRCM 寄存器描述....64
3.1.3.1 SYS_TOP_LDO _SMPS_CTRL_REG....64
3.1.3.2 SYS_EXT_LDO_DIG_LDO_SW_CTRL_REG....66
3.1.3.3 SYS_LFCLK_CTRL_REG....68
3.1.3.4 SYS_HOSC_TYPE_REG....69
3.1.3.5 SYS_RCOSC_CAL_CTRL_REG....69
3.1.3.6 SYS_PLL_CTRL_REG....69
3.1.3.7 SYS_CLK1_CTRL_REG....70
3.1.3.8 SYS_CLK3_CTRL_REG....71
3.1.3.9 DEV_CLK_CTRL_REG....71
3.1.3.10 DCXO_CTRL0_REG....72
3.1.3.11 CONN_BOOT_FLAG_REG....73
3.1.3.12 POWERCTRL_CFG_REG....73
3.1.3.13 SYS1_CTRL_REG....75
3.1.3.14 SYS1_STA_REG....75
3.1.3.15 SYS3_CTRL_REG....76
3.1.3.16 SYS3_STA_REG....76
3.1.3.17 SYS1_WAKEUP_CTRL_REG....77
3.1.3.18 SYS1_SLEEP_CTRL_REG....77
3.1.3.19 DCXO_STABLE_REF_TIME_REG....78
3.1.3.20 DPLL_STABLE_REF_TIME_REG....79
3.1.3.21 LDO_STABLE_REF_TIME_REG....79

3.1.3.22 DIGITAL_SWITCH_REF_TIME_REG....79
3.1.3.23 RTC_LDO_VOL_CTRL_REG....80
3.1.3.24 BG_STABLE_REF_TIME_REG....80
3.1.3.25 DCDC_STABLE_REF_TIME_REG....80
3.1.3.26 BLE_RTC_RST_CTRL_REG....81
3.1.3.27 BLE_RTC_RST_CTRL_REG....81
3.1.3.28 RFAS_CTRL_REG....81
3.1.3.29 AR800A_BOOT_FLAG_REG....82
3.1.3.30 AR800A_BOOT_ADDR_REG....82
3.1.3.31 AR800A_BOOT_ARG_REG....83
3.1.3.32 AR800A_PRIV_REG0....83
3.1.3.33 AR800A_PRIV_REG1....83
3.1.3.34 AR800A_PRIV_REG2....83
3.1.3.35 AR800A_PRIV_REG3....83
3.1.3.36 AR800A_PRIV_REG4....83
3.1.3.37 AR800A_WAKE_TIMER_CNT_REG....83
3.1.3.38 AR800A_WAKE_TIMER_VAL_REG....84
3.1.3.39 AR800A_PRIV_REG5....84
3.1.3.40 AR800A_PRIV_REG6....84
3.1.3.41 AR800A_WAKE_IO_EN_REG....84
3.1.3.42 AR800A_WAKE_IO_DEB_CLK_REG....85
3.1.3.43 AR800A_WAKE_IO_STA_REG....85
3.1.3.44 AR800A_WAKE_IO_STA_REG....85
3.1.3.45 AR800A_IO_WUP_GEN_REG....86
3.1.3.46 AR800A_WAKEUP_IO_DEB_CYCLES_REG....86
3.1.3.47 AR800A_WAKEUP_IO_DEB_CYCLES1_REG....86
3.1.3.48 LDO_MODE_SW_SEL_REG....87
3.1.3.49 SMPS_PARAM_CTRL_REG....87
3.1.3.50 ANA_BG_REG....88
3.1.3.51 DLDO_PARAM_REG....88
3.1.3.52 CFG_IO_ST_REG....89
3.1.3.53 CPU_RST _SRC_REG....89
3.1.3.54 WLAN_HIF_OV_CTRL_REG....90
3.1.3.55 SRAM_BIST_CFG_REG....91
3.1.3.56 WLAN_SRAM_SHARE_REG....91
3.1.3.57 BLE_SRAM_SHARE_CTRL_REG....92
3.1.3.58 LPUART0_WAKEUP_CTRL_REG....92
3.1.3.59 LPUART1_WAKEUP_CTRL_REG....92
3.1.3.60 GPADC_CLK_CTRL_REG....93
3.1.3.61 32K_CLK_CTRL_REG....94
3.1.3.62 WKUP_SRC_BUS_CLK_CTRL_REG....94
3.1.3.63 WKUP_SRC_RST_CTRL_REG....94
3.1.3.64 FLASH_ENCRYPT_AES_NONCE0_REG....95
3.1.3.65 FLASH_ENCRYPT_AES_NONCE1....95

3.1.3.66 BLE_RCOSC_CALIB_REGr0_REG 95
3.1.3.67 BLE_RCOSC_CALIB_REG1 96
3.1.3.68 BLE_CLK32K_SWITCH_REG0 97
3.1.3.69 BLE_CLK32K_SWITCH_REG1 98
3.2 时钟控制单元（CCM） 98
3.2.1 概述 98
3.2.2 CCM 寄存器列表 99
3.2.3 CCM 寄存器描述 99
3.2.3.1 CPU_BUS_CLKCFG_REG 99
3.2.3.2 BUS_CLK_GATING_CTRL_REG 100
3.2.3.3 BUS_DEV_RST_CTRL_REG 102
3.2.3.4 SPI0_CLK_CTRL_REG 105
3.2.3.5 SS_CLK_CTRL_REG 106
3.2.3.6 AUDIO_CLK_CTRL_REG 107
3.2.3.7 IRRX_CLK_CTRL_REG 107
3.2.3.8 IRTX_CLK_CTRL_REG 108
3.2.3.9 SYSTICK_REFCLK_CTRL_REG 109
3.2.3.10 SYSTICK_CALIB_CTRL_REG 110
3.2.3.11 FLASH _SPI_CLK_CTRL_REG 110
3.2.3.12 PCLK_SPC_CLK_CTRL_REG 111
3.2.3.13 PSRAM_OPI_CLK_CTRL_REG 112
3.2.3.14 KEYSCAN_CLK_CTRL_REG 112
3.3 实时时钟(RTC) 113
3.3.1 概述 113
3.3.2 RTC 寄存器列表 113
3.3.3 RTC 寄存器描述 114
3.3.3.1 RTC_ CTRL_REG 114
3.3.3.2 RTC_YYMMDD_REG 115
3.3.3.3 RTC_HHMMSS_REG 115
3.3.3.4 ALM0_CNT_REG 116
3.3.3.5 ALM0_CURVAL_REG 116
3.3.3.6 ALM0_EN_REG 116
3.3.3.7 ALM0_IRQEN_REG 117
3.3.3.8 ALM0_IRQST_REG 117
3.3.3.9 Alarm 1_WK_HHMMSS_REG 117
3.3.3.10 ALM1_EN_REG 118
3.3.3.11 ALM1_IRQEN_REG 119
3.3.3.12 ALM1_IRQST_REG 119
3.3.3.13 ALM_WAKEUP_EN_REG 120
3.3.3.14 FREERUN_CNT_L_REG 120
3.3.3.15 FREERUN_CNT_H_REG 120

3.4 通用定时器(Timer0/1)....121
3.4.1 概述....121
3.4.2 Timer 寄存器列表....121
3.4.3 Timer 寄存器描述....121
3.4.3.1 TMR_IRQ_EN_REG....121
3.4.3.2 TMR_IRQ_STA_REG....122
3.4.3.3 TMR0_CTRL_REG....122
3.4.3.4 TMR0_INTV_VALUE_REG....123
3.4.3.5 TMR0_CUR_VALUE_REG....123
3.4.3.6 TMR1_CTRL_REG....124
3.4.3.7 TMR1_INTV_VALUE_REG....125
3.4.3.8 TMR1_CUR_VALUE_REG....125
3.5 看门狗定时器(Watchdog)....125
3.5.1 概述....125
3.5.2 Watchdog 寄存器列表....125
3.5.3 Watchdog 寄存器描述....126
3.5.3.1 WDOG_IRQ_EN_REG....126
3.5.3.2 WDOG_IRQ_EN_REG....126
3.5.3.3 WDOG_CTRL_REG....126
3.5.3.4 WDOG_CFG_REG....127
3.5.3.5 WDOG_MODE_REG....127
3.5.3.6 WDOG_OUTPUT_CTRL_REG....128
4 DMA 控制器....129
4.1 安全 DMA (SDMA)....129
4.1.1 概述....129
4.1.2 SDMA 寄存器列表....129
4.1.3 SDMA 寄存器描述....129
4.1.3.1 SDMA_IRQ_EN_REG....129
4.1.3.2 SDMA_IRQ_PEND_STA_REG....130
4.1.3.3 SDMA_AUTO_GAT_REG....131
4.1.3.4 SDMA_CTRL_REG....131
4.1.3.5 SDMA_SRC_ADDR_REG....133
4.1.3.6 SDMA_DEST_ADDR_REG....133
4.1.3.7 SDMA_BC_REG....134
4.2 非安全 DMA (NDMA)....134
4.2.1 概述....134
4.2.2 NDMA 寄存器列表....134
4.2.3 NDMA 寄存器描述....135

4.2.3.1 NDMA_IRQ_EN_REG 135
4.2.3.2 NDMA_IRQ_PEND_STA_REG 136
4.2.3.3 NDMA_AUTO_GAT_REG 138
4.2.3.4 NDMA_CTRL_REG 139
4.2.3.5 NDMA_SRC_ADDR_REG 141
4.2.3.6 NDMA_DEST_ADDR_REG 141
4.2.3.7 NDMA_BC_REG 141
5 安全模块 143
5.1 加解密算法加速器(Crypto Engine) 143
5.1.1 概述 143
5.1.2 Crypto Engine 寄存器列表 144
5.1.3 Crypto Engine 寄存器描述 145
5.1.3.1 CE_CTL_REG 145
5.1.3.2 CE_KEY[n]_REG 147
5.1.3.3 CE_IV [n]_REG 147
5.1.3.4 CE_CNT[n]_REG 147
5.1.3.5 CE_FCSR_REG 147
5.1.3.6 CE_ICSR_REG 148
5.1.3.7 CE_MD [n]_REG 149
5.1.3.8 CE_CTS_LEN_REG 150
5.1.3.9 CE_CRC_POLY_REG 150
5.1.3.10 CE_RESULT_REG 150
5.1.3.11 CE_MD[n]_REG 150
5.1.3.12 CE_RX_REG 150
5.1.3.13 CE_TX_REG 150
5.1.4 CE 模块时钟要求 151
5.2 真随机数发生器(TRNG) 151
5.2.1 概述 151
5.2.2 TRNG 寄存器列表 151
5.2.3 TRNG 寄存器描述 152
5.2.3.1 TRNG_CTL_REG 152
5.2.3.2 TRNG_JITTER_REG 153
5.2.3.3 TRNG_JITTER_CNT_TIMING_REG 154
5.2.3.4 TRNG_MONITOR_RCT_REG 154
5.2.3.5 TRNG_MONITOR_APT_REG 154
5.2.3.6 TRNG_EXSTRACT_CFG_REG 155
5.2.3.7 TRNG_RAND_BIT_URN0_REG 155
5.2.3.8 TRNG_RAND_BIT_URN1_REG 155
5.2.3.9 TRNG_RAND_BIT_URN2_REG 156
5.2.3.10 TRNG_RAND_BIT_URN3_REG 156
5.2.3.11 TRNG_JITTER_CNT_RESULT0_REG 156

5.2.3.12 TRNG_JITTER_CNT_RESULT1_REG....156
5.2.3.13 TRNG_JITTER_CNT_RESULT2_REG....156
5.2.3.14 TRNG_JITTER_CNT_RESULT3_REG....157
5.2.3.15 TRNG_JITTER_CNT_RESULT4_REG....157
5.2.3.16 TRNG_JITTER_CNT_RESULT5_REG....157
5.2.3.17 TRNG_JITTER_CNT_RESULT6_REG....157
5.2.3.18 TRNG_JITTER_CNT_RESULT7_REG....158
5.2.3.19 TRNG_JITTER_COUNTER_READY_REG....158
5.2.3.20 TRNG_REG_ACCESS_CTR1....158
5.2.3.21 TRNG_REG_ACCESS_CTR2....158
5.3 安全标识(Security ID)....159
5.3.1 概述....159
5.3.2 SID 寄存器列表....159
5.3.3 SID 寄存器描述....159
5.3.3.1 SID_PR_CTRL_REG....159
5.3.3.2 SID_PKEY_REG....160
5.3.3.3 SID_RKEY_REG....160
5.3.3.4 SID_BURN_TIMING_REG....161
5.3.3.5 SID_DBG_REG....161
5.3.3.6 SID_VALUE_REG....161
6 外设及通用接口模块....162
6.1 外设安全控制(TZASC)....162
6.1.1 概述....162
6.1.2 TZASC 寄存器列表....162
6.1.3 TZASC 寄存器描述....163
6.1.3.1 AHB_DEV_SEC_CTRL_REG....163
6.1.3.2 APB_DEV_SEC_CTRL_REG....165
6.1.3.3 TZASC_INT_EN_REG....167
6.1.3.4 TZASC_INT_STA_REG....167
6.1.3.5 SEC_SPACE_ADRR_START_REG....167
6.1.3.6 SEC_SPACE_ADRR_END_REG....167
6.1.3.7 FLASHCTRL_SEC_CTRL_REG....168
6.1.3.8 FLASH_PSRAM_SEC_SPACE_ADRR_START_REG....168
6.1.3.9 FLASH_PSRAM_SEC_SPACE_ADRR_END_REG....168
6.1.3.10 TZASC_CLK_MANAGE_SEC_CASE_REG....169
6.2 UART 接口....170
6.2.1 概述....170
6.2.2 UART 寄存器列表....171
6.2.3 UART 寄存器描述....172
6.2.3.1 UART_RBR_REG....172

6.2.3.2 UART_THR_REG....172
6.2.3.3 UART_DLL_REG....173
6.2.3.4 UART_DLH_REG....173
6.2.3.5 UART_IER_REG....173
6.2.3.6 UART_IIR_REG....175
6.2.3.7 UART_FCR_REG....176
6.2.3.8 UART_LCR_REG....177
6.2.3.9 UART_MCR_REG....179
6.2.3.10 UART_LSR_REG....180
6.2.3.11 UART_MSR_REG....182
6.2.3.12 UART_SCH_REG....184
6.2.3.13 UART_USR_REG....185
6.2.3.14 UART_TFL_REG....186
6.2.3.15 UART_RFL_REG....186
6.2.3.16 UART_RBR_REG....186
6.2.3.17 UART_TXDLY_REG....188
6.2.3.18 UART_BDC_REG....188
6.2.3.19 UART_BDCL_REG....188
6.2.3.20 UART_ABCR_REG....189
6.3 LPUART 接口....189
6.3.1 概述....189
6.3.2 LPUART 寄存器列表....189
6.3.3 LPUART 寄存器描述....190
6.3.3.1 LUART_GP_SR_CON_REG....190
6.3.3.2 LUART_BAUD_CONFIG_REG....190
6.3.3.3 LUART_RX_CONFIG_REG....190
6.3.3.4 LUART_RX_DATA_REG....191
6.3.3.5 LUART_INTR_EN_REG....192
6.3.3.6 LUART_INTR_STATUS_REG....192
6.3.3.7 LUART_INTR_CLR_REG....192
6.3.3.8 LUART_RX_CMP_REG1....193
6.3.3.9 LUART_RX_CMP_REG2....193
6.4 SPI 接口....194
6.4.1 概述....194
6.4.2 SPI 寄存器列表....195
6.4.3 SPI 寄存器描述....196
6.4.3.1 SPI_VER_REG....196
6.4.3.2 SPI_CTRL_REG....196
6.4.3.3 SPI_TCTRL_REG....197
6.4.3.4 SPI_IER_REG....199
6.4.3.5 SPI_STA_REG....201

6.4.3.6 SPI_FCTL_REG 203
6.4.3.7 SPI_FST_REG 204
6.4.3.8 SPI_WAIT_REG 205
6.4.3.9 SPI_CCTR_REG 206
6.4.3.10 SPI_BC_REG 207
6.4.3.11 SPI_TC_REG 207
6.4.3.12 SPI_BCC_REG 207
6.4.3.13 SPI_NDMA_MODE_CTRL_REG 208
6.4.3.14 SPI_TXD_REG 208
6.4.3.15 SPI_RXD_REG 209
6.5 TWI 接口 209
6.5.1 概述 209
6.5.2 TWI 寄存器列表 210
6.5.3 TWI 寄存器描述 211
6.5.3.1 TWI_ADDR_REG 211
6.5.3.2 TWI_XADDR_REG 211
6.5.3.3 TWI_DATA_REG 212
6.5.3.4 TWI_ADDR_REG 212
6.5.3.5 TWI_STAT_REG 214
6.5.3.6 TWI_CCR_REG 215
6.5.3.7 TWI_SRST_REG 215
6.5.3.8 TWI_EFR_REG 215
6.5.3.9 TWI_LCR_REG 216
6.6 CIR 接口 217
6.6.1 概述 217
6.6.1.1 CIR 接收控制器（IRRX） 217
6.6.1.2 CIR 发射控制器（IRTX） 217
6.6.2 CIR 寄存器列表 218
6.6.3 CIR Receiver 寄存器描述 219
6.6.3.1 CIR_CTL_REG 219
6.6.3.2 CIR_RXCTL_REG 220
6.6.3.3 CIR_RXFIFO_REG 220
6.6.3.4 CIR_RXINT_REG 220
6.6.3.5 CIR_RXSTA_REG 221
6.6.3.6 CIR_CONFIG_REG 222
6.6.4 CIR Transmit 寄存器描述 223
6.6.4.1 CIR_TGLR_REG 223
6.6.4.2 CIR_X_REG 224
6.6.4.3 CIR_TCR_REG 224
6.6.4.4 CIR_IDC_H_REG 225

6.6.4.5 CIR_IDC_L_REG 225
6.6.4.6 CIR_TICR_H_REG 225
6.6.4.7 CIR_TICR_L_REG 226
6.6.4.8 CIR_TEL_REG 226
6.6.4.9 CIR_TXINT_REG 226
6.6.4.10 CIR_TAC_REG 227
6.6.4.11 CIR_TXSTA_REG 227
6.6.4.12 CIR_TXT_REG 228
6.6.4.13 CIR_DMA_CTL_REG 228
6.6.4.14 CIR_TXFIFO_REG 229
6.7 PWM 接口 229
6.7.1 概述 229
6.7.2 PWM 寄存器列表 230
6.7.3 PWM 寄存器描述 231
6.7.3.1 PWM_PIER_REG 231
6.7.3.2 PWM_PISR_REG 232
6.7.3.3 PWM_CIER_REG 233
6.7.3.4 PWM_CISR_REG 235
6.7.3.5 PWM_PCCR01_REG 239
6.7.3.6 PWM_PCCR23_REG 239
6.7.3.7 PWM_PCCR45_REG 240
6.7.3.8 PWM_PCCR67_REG 241
6.7.3.9 PWM_PDZCR01_REG 242
6.7.3.10 PWM_PDZCR23_REG 242
6.7.3.11 PWM_PDZCR45_REG 243
6.7.3.12 PWM_PDZCR67_REG 243
6.7.3.13 PWM_PER_REG 243
6.7.3.14 PWM_CER_REG 244
6.7.3.15 PWM_PCR_REG 245
6.7.3.16 PWM_PPR_REG 246
6.7.3.17 PWM_PCNTR_REG 247
6.7.3.18 PWM_CCR_REG 247
6.7.3.19 PWM_CRLR_REG 247
6.7.3.20 PWM_CFLR_REG 248
6.8 智能卡接口(ISO7816) 248
6.8.1 概述 248
6.8.2 功能描述 249
6.8.2.1 模块框图 249
6.8.2.2 接口信号 249
6.8.2.3 管脚应用电路 249

6.8.2.4 电气特性 250
6.8.2.5 SCR 冷复位 250
6.8.2.6 SCR 热复位 251
6.8.3 ISO7816 寄存器列表 251
6.8.4 ISO7816 寄存器描述 252
6.8.4.1 SCR_CSR_REG 252
6.8.4.2 SCR_INTEN_REG 254
6.8.4.3 SCR_INTST_REG 255
6.8.4.4 SCR_FCSR_REG 257
6.8.4.5 SCR_FIFOCNT_REG 258
6.8.4.6 SCR_REPEAT_REG 258
6.8.4.7 SCR_CLKDIV_REG 258
6.8.4.8 SCR_LTIM_REG 259
6.8.4.9 SCR_CTIM_REG 259
6.8.4.10 SCR_LCTLR_REG 260
6.8.4.11 SCR_FSM_REG 260
6.8.4.12 SCR_DT_REG 261
6.8.4.13 SCR_FIFO_REG 261
6.8.4.14 SCR_VER_REG 261
6.9 通用模数转换器(GPADC) 261
6.9.1 概述 261
6.9.2 功能描述 262
6.9.2.1 模块框图 262
6.9.2.2 接口信号 263
6.9.2.3 工作模式 263
6.9.3 GPADC 寄存器列表 264
6.9.4 GPADC 寄存器描述 264
6.9.4.1 GP_SR_CON_REG 264
6.9.4.2 GP_CTRL_REG 265
6.9.4.3 GP_CS_EN_REG 266
6.9.4.4 GP_FIFO_INTC_REG 266
6.9.4.5 GP_FIFO_INTS_REG 267
6.9.4.6 GP_FIFO_DATA_REG 268
6.9.4.7 GP_CDATA_REG 268
6.9.4.8 GP_DATAL_INTC_REG 268
6.9.4.9 GP_DATAH_INTC_REG 268
6.9.4.10 GP_DATA_INTC_REG 268
6.9.4.11 GP_DATAL_INTS_REG 269
6.9.4.12 GP_DATAH_INTS_REG 269
6.9.4.13 GP_DATA_INTS_REG 269

6.9.4.14 GP_CHn_CMP_DATA_REG 269
6.9.4.15 GP_CHn_DATA_REG 270
6.10 通用 I/O(GPIO) 270
6.10.1 概述 270
6.10.2 GPIO 功能描述 271
6.10.3 GPIO 寄存器列表 274
6.10.4 GPIO 寄存器描述 275
6.10.4.1 Pn_CFG0_REG 275
6.10.4.2 Pn_CFG1_REG 275
6.10.4.3 Pn_CFG2_REG 276
6.10.4.4 Pn_CFG3_REG 276
6.10.4.5 Pn_DATA_REG 276
6.10.4.6 Pn_DRV0_REG 276
6.10.4.7 Pn_DRV1_REG 277
6.10.4.8 Pn_PULL0_REG 277
6.10.4.9 Pn_PULL1_REG 277
6.10.4.10 Pn_EINT_CFG0_REG 277
6.10.4.11 Pn_EINT_CFG1_REG 278
6.10.4.12 Pn_EINT_CFG2_REG 278
6.10.4.13 Pn_EINT_CFG3_REG 278
6.10.4.14 Pn_EINT_CTRL_REG 279
6.10.4.15 Pn_EINT_STA_REG 279
6.10.4.16 Pn_EINT_DBC_REG 279
7 音频接口(Audio) 280
7.1 数字音频功放驱动器(Audio-PWM) 280
7.1.1 概述 280
7.1.2 功能描述 280
7.1.2.1 模块框图 280
7.1.2.2 接口信号 280
7.1.2.3 时钟复位及中断说明 281
7.1.2.4 典型应用图示 282
7.1.3 Audio-PWM Class-D Driver 寄存器列表 282
7.1.4 Audio-PWM Class-D Driver 寄存器描述 283
7.1.4.1 CLD_DIG_CTRL_REG 283
7.1.4.2 CLD_FIFO_CTRL_REG 285
7.1.4.3 CLD_FIFO_STA_REG 286
7.1.4.4 AC_CLD_TXDATA_REG 287
7.1.4.5 CLD_TXCNT_REG 287
7.2 数字音频接口控制器(DAUDIO) 287

7.2.1 概述 287
7.2.2 功能描述 288
7.2.2.1 模块框图 288
7.2.2.2 接口信号 288
7.2.2.3 时钟源 289
7.2.2.4 时序说明 289
7.2.2.5 软件操作 290
7.2.2.6 电气特性 291
7.2.3 DAUDIO 寄存器列表 292
7.2.4 DAUDIO 寄存器描述 293
7.2.4.1 DA_CTRL_REG 293
7.2.4.2 DA_FMT0_REG 294
7.2.4.3 DA_CTRL_REG 296
7.2.4.4 DA_ISTA_REG 297
7.2.4.5 DA_RXFIFO_REG 298
7.2.4.6 DA_FCTL_REG 298
7.2.4.7 DA_FSTA_REG 299
7.2.4.8 DA_INT_REG 300
7.2.4.9 DA_TXFIFO_REG 301
7.2.4.10 DA_CLKD_REG 301
7.2.4.11 DA_TXCNT_REG 302
7.2.4.12 DA_RXCNT_REG 302
7.2.4.13 DA_CHCFG_REG 302
7.2.4.14 DA_TXnCHSEL_REG 303
7.2.4.15 DA_TXnCHMAP_REG 304
7.2.4.16 DA_RXCHSEL_REG 305
7.2.4.17 DA_RXCHMAP_REG 305
8 常见问题说明 308
附录 A： 术语表 309

图片目录

图 5-1 CE 模块内部框架图 143
图 5-2 TRNG 模块数据流框架图 151
图 6-1 UART 串行数据时序图 170
图 6-2 UART IrDA 时序图 170
图 6-3 SPI Modes with Clock Polarity and Phase 194
图 6-4 SPI Phase 0 Transfer Format 194
图 6-5 SPI Phase 1 Transfer Format 195
图 6-6 TWI 时序图 210
图 6-7 IRTX 调制技术示例 218
图 6-8 IRTX NEC 协议示例 218
图 6-9 SCR 逻辑框图 249
图 6-10 SCR IO Pad 框图 249
图 6-11 SCR 冷复位时序框图 250
图 6-12 SCR 热复位时序框图 251
图 6-13 GPADC 逻辑框图 262
图 7-1 Audio-PWM Class-D 驱动器逻辑框图 280
图 7-2 Audio-PWM Class-D 驱动器时钟系统 281
图 7-3 Audio-PWM Class-D 驱动器复位系统 281
图 7-4 Audio-PWM Class-D 驱动器中断系统 282
图 7-5 Audio-PWM Class-D 驱动器应用框图 282
图 7-6 DAudio 内部逻辑框图 288
图 7-7 标准 I2S/TDM-I2S 模式时序 289
图 7-8 左对齐/TDM-Left 模式时序 290
图 7-9 右对齐/TDM-Right 模式时序 290
图 7-10 DAI 主模式时序图 291
图 7-11 DAI 从模式时序图 292

表格目录

表 6-1 UART 中断 ID 优先级.....175
表 6-2 SCR 接口信号.....249
表 6-3 SCR 冷复位时序要求.....250
表 6-4 SCR 热复位时序要求.....251
表 6-5 GPADC 接口信号.....263
表 6-6 XR806Bxxx GPIO 复用关系表.....271
表 6-7 XR806Axxx GPIO 复用关系表.....274
表 7-1 Audio-PWM 接口信号.....280
表 7-2 DAudio 接口信号.....289
表 7-3 DAI 时钟源.....289
表 7-4 DAI 主模式时序要求.....291
表 7-5 DAI 主模式时序要求.....292
表 A-1 术语表.....309

1 前言

1.1 文档简介

本文档介绍了关于 XR806 的具体信息，包括微控制器、存储器、外设模块的功能和寄存器信息的完整描述。芯片的管脚描述、电气特性和封装信息等可以从 XR806 Datasheet 获取。

1.2 目标读者

使用 XR806 的应用开发人员。

1.3 适用范围

此文档适用于支持 XR806 系列所有芯片产品。

1.4 文档约定

1.4.1 标志说明

本文档采用各种醒目的标志来表示在操作过程中应该特别注意的地方，这些标志的含义如下：

标识	说明
 警告	该标志后的说明应给予格外关注，如果不遵守，可能会导致人员受伤或死亡。
 注意	提醒操作中应注意的事项。不当的操作可能会损坏器件，影响可靠性、降低性能等。
 说明	为准确理解文中指令、正确实施操作而提供的补充或强调信息。
 窍门	一些容易忽视的小功能、技巧。了解这些功能或技巧能帮助解决特定问题或者节省操作时间。

1.4.2 地址与数据描述方法约定

本文档在描述地址、数据时遵循如下约定：

符号	例子	说明
0x	0x0200，0x79	地址或数据以 16 进制表示。
0b	0b010，0b00 000 111	数据采用二进制表示(寄存器描述除外)。
X	00X，XX1	数据描述中，X 代表 0 或 1。 例如，00X 代表 000 或 001；XX1 代表 001，011，101 或 111。

1.4.3 数值单位约定

本文档在描述数据容量（如 NAND 容量）时，单位词头代表的是 1024 的倍数；描述频率、数据速率等时则代表的是 1000 的倍数。具体如下：

类型	符号	对应数值
数据容量（如 NAND 容量）	1 K	1024
	1 M	1 048 576
	1 G	1 073 741 824
频率，数据速率等	1 k	1000
	1 M	1 000 000
	1 G	1 000 000 000

2 系统和存储

2.1 XR806 应用子系统

2.1.1 概述

XR806 应用子系统采用了带有 Trustzone-M 功能的 Cortex M33 Star 微控制器（ARMv8-M 架构），支持时钟频率从 32KHz 到 160MHz，集成了 320KB SRAM 和 160KB ROM，同时支持通过 SQPI 接口扩展外部 Flash 容量至最高 16MB，允许代码直接从 Flash 和 PSRAM 内执行，允许读写数据在 PSRAM 中。它还包括许多外围设备，包括 UART, TWI, SPI, PWM, IrDA (T/R)和 GPADC 等。

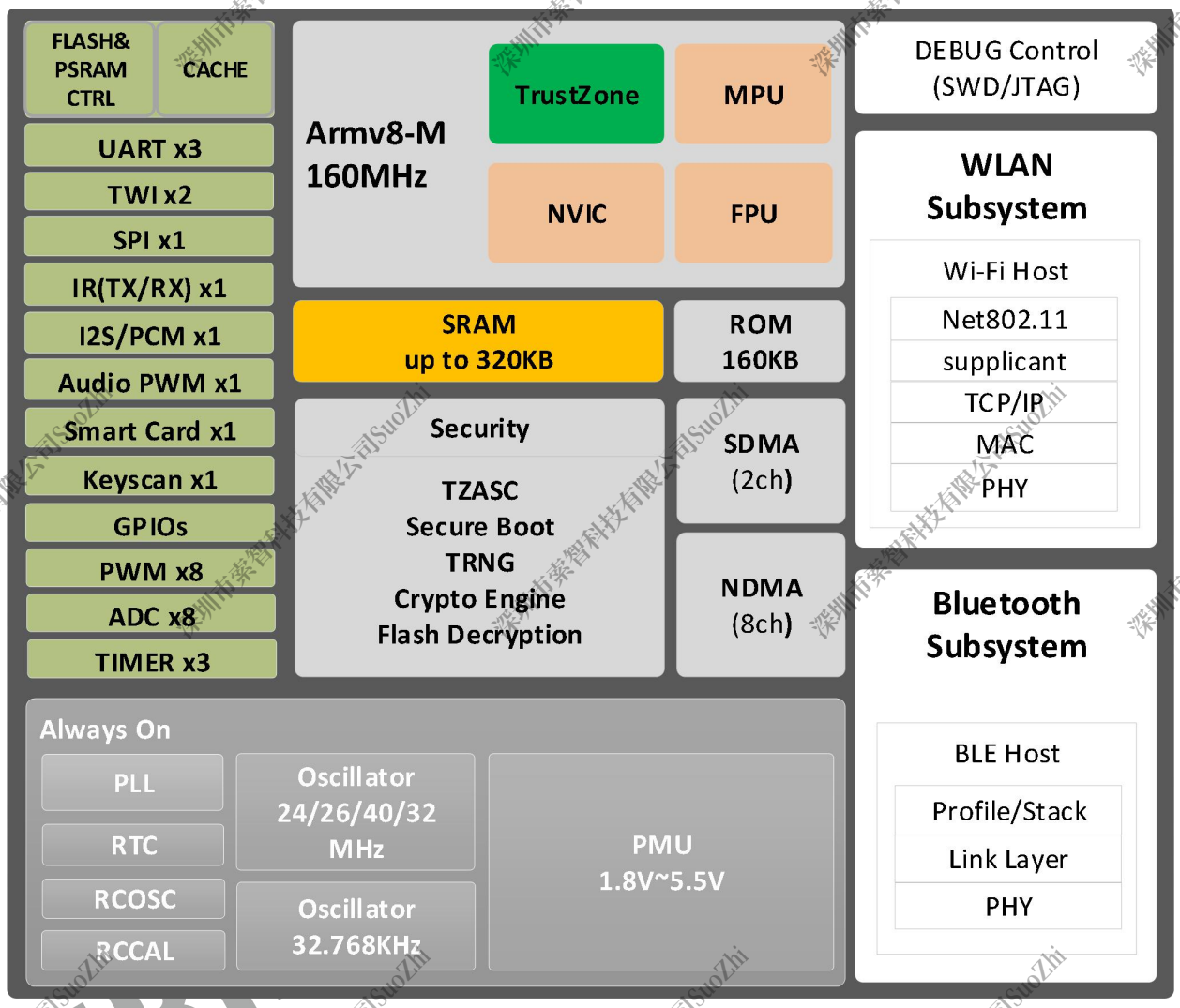
Wi-Fi 子系统包含 802.11b/g/n 基带、MAC、集成了 PA、LNA、Switch 及谐波滤波器的射频部分，可以满足低功耗、高集成度和高性能的网络应用。采用 XRADIOTECH MPD™ 技术设计了一种新型的数字射频发射机，以提供更高的输出功率并保持较高的发射效率，同时保持芯片对天线失配不那么敏感，使得在不同驻波比下始终具有良好的 EVM。

蓝牙子系统包含 Bluetooth 5.0 标准的全部特性，包括射频、调制解调器、基带和规范等。针对长距离和低功耗的应用特别是智能家庭网格连接做了专门优化，高性能和更大的 SRAM 允许简单的组网网关设计与集成的 Wi-Fi 系统直接连接到互联网。

为低功耗嵌入式网络应用而设计的 SoC，集成了网络处理器，包含了大量 TCP/IP 协议的 IPv4/IPv6 基础服务集。可以通过连接到外部主机 CPU 的串行 UART/SPI 链路访问这些服务。

2.1.2 功能描述

2.1.2.1 系统框图



2.1.2.2 关键特性

特性	描述		XR806AF2L	XR806BF2L	XR806BM2I
Package	Trays and tape-in-reel		4x4mm^2	5x5mm^2	5x5mm^2
			QFN32	QFN40	QFN40
Supply voltage	Power supply from system		1.8~5.5V		
	5V IO		Yes		
PMU	LDO for external device (EXT LDO)		Yes		
Clock	External HOSC		24/26/32/40MHz		
	External LOSC		32.768KHz		
	Internal RCOSC		30~60KHz		
	Internal RCOSC Calibration		YES		
MCU Core	Core Type		Cortex M33 Star (Armv8-M Architecture)		
	Core clock maximum frequency		160MHz	160MHz	up to 240MHz
Memory	Internal ROM		160KB		
	Internal RAM		up to 320KB		
	Internal Flash with XIP		2MB	2MB	-
	External Flash with XIP		Max. 16MB		
	Internal PSRAM		-	-	2MB
Backup register	Backup register for power save		16B		
Secure boot	-		Yes		
Trustzone-M	Default size: 28KB		Yes		
Crypto Engine	AES, DES, 3DES, SHA-1, MD5, TRNG, CRC32/16, SHA256		Yes		
TRNG	Provide random number seed		Yes		
WDG reset protection	Protect specified peripherals been reset by watchdog reset		Yes		
BOR	BOR Detection		Yes		
Wi-Fi	802.11 b/g/n		Yes		
Bluetooth	BLE 5.0		Yes		
	BLE Configure		Yes		
	BLE Mesh		Yes	Yes	Yes
Peripheral	1.8/3.3/5V GPIO	General Purpose	4	4	4

特性	描述		XR806AF2L	XR806BF2L	XR806BM2I
	1.8/3.3 GPIO	General Purpose	14	22	22
	WAKEUP IO	From RTC wake-up	8	10	10
	UART	Max.3Mbps	3	3	3
	SPI	Master and slave	1	1	1
	I2C	Max.400Kbps	2	2	2
	IR	TX and RX	1	1	1
	DAudio	IIS/PCM	1	1	1
	Audio PWM	Playback Channel	1	1	1
	PWM	Output Channel	8	8	8
	KEYSCAN	8*16	-	YES	YES
	Smart Card	ISO7816	1	1	1
	GPADC	VBAT channel	1	1	1
		Normal channel	3	7	7
	NDMA	8 Channel	YES	YES	YES
	SDMA	2 Channel	YES	YES	YES
	Timer	RTC timer	1	1	1
		Watchdog timer	1	1	1
		Normal timer	2	2	2
		Wakeup timer	1	1	1

2.1.2.3 NVIC 寄存器列表

关于系统控制、系统定时器（System Tick）、可嵌套中断向量（NVIC）等详细信息的描述，可参考《ARM Cortex-M33 Technology Reference Manual》。以下仅对中断向量部分做简要描述。

Module Name	**Base Address**	
Nested Vectored Interrupt Controller	0xE000E000	
Register Name	**Offset Address**	**Description**
SYSTICK_CTRL	0x0010	SysTick Control and Status Register
SYSTICK_RELOAD	0x0014	SysTick Reload Value Register
SYSTICK_CURVAL	0x0018	SysTick Current Value Register
NVIC_ISER0 – NVIC_ISER7	0x0100 – 0x011C	Interrupt Set-Enable Registers
NVIC_ICER0 – NVIC_ICER7	0x0180 – 0x019C	Interrupt Clear-Enable Registers
NVIC_ISPR0 – NVIC_ISPR7	0x0200 – 0x021C	Interrupt Set-Pending Registers
NVIC_ICPR0 – NVIC_ICPR7	0x0280 – 0x029C	Interrupt Clear-Pending Registers
NVIC_IABR0 – NVIC_IABR7	0x0300 – 0x031C	Interrupt Active Bit Registers
NVIC_IPR0 – NVIC_IPR59	0x0400 – 0x04CF	Interrupt Priority Registers
SCB	0x0D08 – 0x0D3f	System Control Block

2.1.3 中断寄存器描述

中断号	向量	中断源	优先级	描述
0	0x00	-	-	Stack top is loaded from first entry of vector table on reset.
1	0x04	-	-3	Reset
2	0x08	-	-2	NMI
3	0x0C	-	-1	Hardware Fault
4	0x10	-	configurable	Memory Management
5	0x14	-	configurable	Bus Fault
6	0x18	-	configurable	Usage Fault
7	0x1C	-	-	-
8	0x20	-	-	-
9	0x24	-	-	-
10	0x28	-	-	-
11	0x2C	-	configurable	SVCall
12	0x30	-	configurable	Debug Monitor
13	0x34	-	-	-
14	0x38	-	configurable	PendSV
15	0x3C	-	configurable	System Tick
16	0x40	DMA	configurable	Direct Memory Access Controller
17	0x4C	MSGBOX	configurable	Message Box(IRQ0)
18	0x50	UART0	configurable	UART Controller 0
19	0x54	UART1	configurable	UART Controller 1
20	0x58	SPI0	configurable	SPI Controller 0
21	0x60	TWI0	configurable	TWI Controller 0
22	0x64	TWI1	configurable	TWI Controller 1
23	0x68	WDT	configurable	Watchdog
24	0x6C	TIMER0	configurable	Timer 0
25	0x70	TIMER1	configurable	Timer 1
26	0x74	ALARM0	configurable	Alarm 0
27	0x78	ALARM1	configurable	Alarm 1

28	0x80	DAUDIO	configurable	Digital Audio Controller
29	0x84	PWM/ECT	configurable	PWM/ECT Controller
30	0x88	SS	configurable	Secure System Controller
31	0x8C	GPADC	configurable	GPADC Controller
32	0x90	GPIOB	configurable	GPIO Controller Port B
33	0x98	IRRX	configurable	IR Receiver
34	0x9C	IRTX	configurable	IR Transmitter
35	0XA4	A-WUP	configurable	APP Wake Up(Timer & IO)
36	0xA8	FLASHC	configurable	FLASH Controller
37	0XAC	UART2	configurable	UART Controller 2
38	0XB4	WLAN	configurable	WLAN
39	0XB8	Audio PWM	configurable	AUDIO PWM
40	0XC0	AVS	configurable	AVS psensor
41	0XCC	BLE_LL	configurable	BLE_LL
42	0XD0	BTCOEX	configurable	BTCOEX
43	0XD4	KEYSCAN	configurable	Key scan controller
44	0XD8	SMCARD	configurable	ISO7816 SIM CARD interface
45	0XDC	DMA_SEC	configurable	Secure DMA memory access controller
46	0XE4	LPUART0	configurable	LPUART0 wakeup controller
47	0XE8	LPUART1	configurable	LPUART1 wakeup controller
48	0XEC	SEC_FAULT	configurable	Security access fault case
49	0XF0	RCCAL	configurable	RCOSC calibration

说明

1. 详细信息请参考《ARM Cortex-M33 Technology Reference Manual》。

2.2 系统控制模块（SYSCTRL）

2.2.1 概述

系统控制模块主要包含了部分 SIP FLASH/PSRAM PIN Mapping、Psensor、Debug Register 等信息。

2.2.2 SYSCTRL 寄存器列表

模块名	**基地址**	
System Control	0x4000A000	
寄存器名	**偏移地址**	**描述**
SIP_FLASH_TEST_MAP_REG	0x0044	SIP FLASH Test Mapping Register
PS_CTL_REG	0x0050	Psensor control register
PS_CNT_REG	0x0054	Psensor counter register
FLASH_PSARM_PIN_MAP_REG	0x0060	FLASH/PSRAM PIN Mapping Control Register
GENERAL_DBG0_REG	0x00B0	General Debug 0 Register
GENERAL_DBG1_REG	0x00B4	General Debug 1 Register

2.2.3 SYSCTRL 寄存器描述

2.2.3.1 SIP_FLASH_TEST_MAP_REG

偏移地址 : 0x0044			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	RW	0x0	0x429d: SIP_FLASH_TEST/ SIP_PSRAM _TEST filed is writable other: SIP_FLASH_TEST/ SIP_PSRAM _TEST filed is read only Note: The field of SIP_FLASH_TEST/SIP_PSRAM_TEST only can be changed when these bits are set to 0x429D. In one write operation, the GRPCM will check this field whether equals to 0x429D. If not, the value of SIP_FLASH_TEST/SIP_PSRAM_TEST will be ignored. This field is always read with value 0x0000. Examples: After write 0x429d0001, then read value = 0x00000001 After write 0x11110000, then read value = 0x00000001 After write 0x429d0000, then read value = 0x00000000
15:1	/	/	/
0	RW	0x0	SIP_FLASH_TEST 0: SIP FLASH IOs mapping is disabled 1: SIP FLASH IOs are mapped to the external flash PINs

2.2.3.2 PS_CTL_REG

偏移地址: 0x0050			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:17	/	/	/
16	RW1C	0x0	CLK250M_CNT_RDY clk250M counter ready 0: not finish 1:finish
15:11	/	/	/
10:8	R/W	0x0	PS_DEV_SEL psensor device sel 000: select psensor_0 001: select psensor_1 Others: reserved
7:6	/	/	/
5:4	R/W	0x0	PS_EN_SEL OSC select 00:disable(no dynamic power) 01 : rvt_casecode ring osc 10: lvt_casecode ring osc 11:rvt_normal ring osc
3:1	R/W	0x0	PS_N_PRD clk num period. 0: 4 --- 2/13 us (26M HOSC), 0.1us (40M HOSC) 1: 8 --- 4/13 us (26M HOSC) , 0.2us (40M HOSC) 2: 16---8/13 us (26M HOSC) , 0.4us (40M HOSC) 3: 32---16/13us (26M HOSC) , 0.8us (40M HOSC) 4: 64—32/13 us (26M HOSC) , 1.6us (40M HOSC) 5: 128—64/13 us (26M HOSC) , 3.2us (40M HOSC) 6: 256—128/13us (26M HOSC) , 6.4us (40M HOSC) 7: 512—256/13us (26M HOSC) , 12.8us (40M HOSC)
0	R/W	0x0	PS_EN psensor Enable. 0: disable 1: psensor enable

2.2.3.3 PS_CNT_REG

偏移地址 ：0x0054			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15:0	R	0x0	CLK250M_CNT clk 250M counter

2.2.3.4 FLASH_PSARM_PIN_MAP_REG

地址 ：0x0060			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	/
25:24	RW	0x0	mode_5vbias Mode control of 5V IO for PB0/1/14/15
23:18	/	/	/
17:16	RW	0x2	FLASH_PSARM_PIN_MAP1 When Flash/Psram access on GPIOB08~GPIOB11 PINs， which controller Chip Select (CS) is corresponding 0: reserved 1: only CS0 of Flash/Psram controller 2: only CS1 of Flash/Psram controller 3: both CS0 and CS1 of Flash/Psram controller
15:2	/	/	/
1:0	RW	0x1	FLASH_PSARM_PIN_MAP0 When Flash/Psram access on GPIOB02~GPIOB05 PINs， which controller Chip Select (CS) is corresponding 0: reserved 1: only CS0 of Flash/Psram controller 2: only CS1 of Flash/Psram controller 3: both CS0 and CS1 of Flash/Psram controller

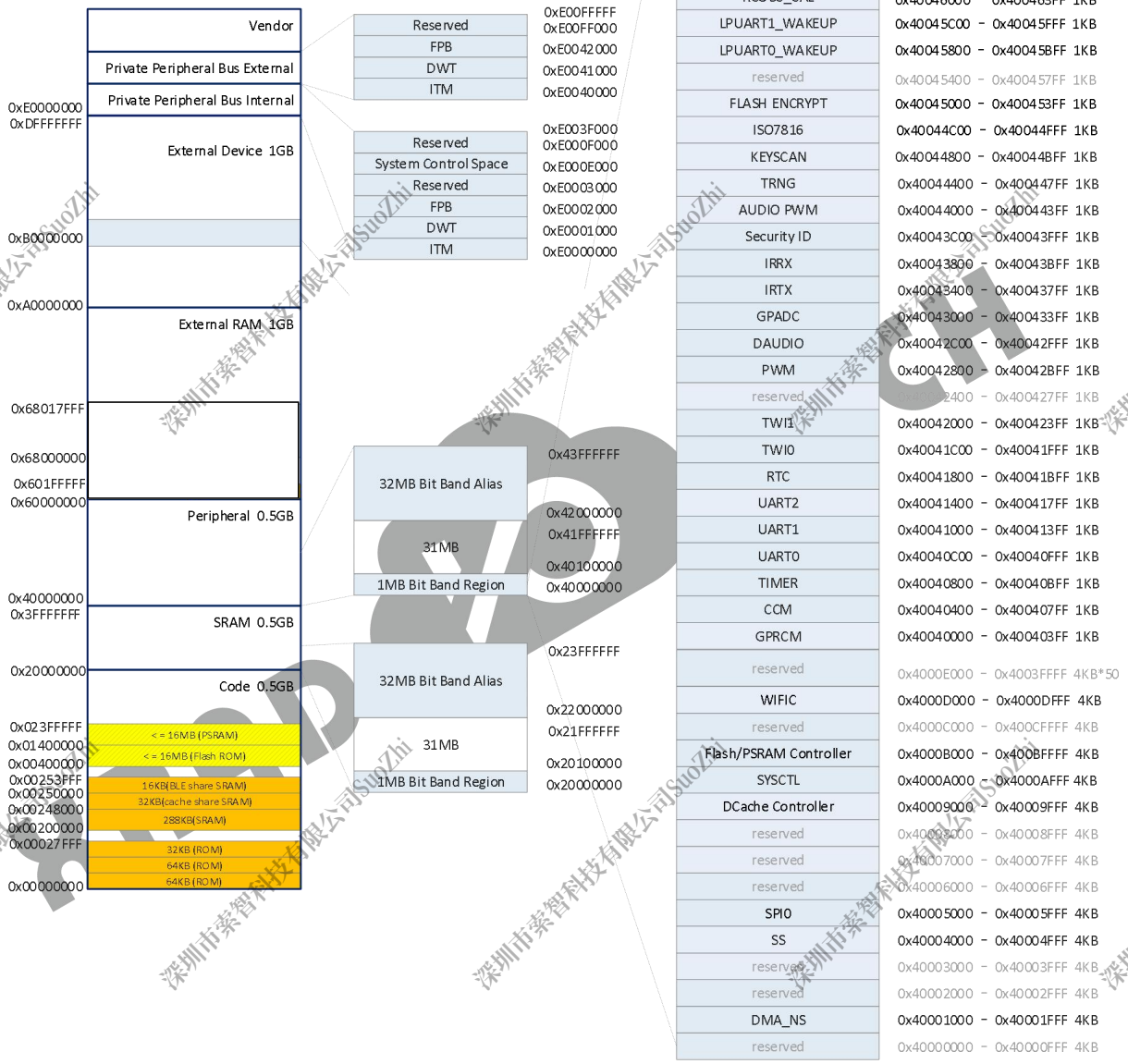
2.2.3.5 GENERAL_DBG0_REG

偏移地址 ：0x00B0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:00	RW	0	GENERAL_DBG0 General debug register 0 is used for storing flag or some data

2.2.3.6 GENERAL_DBG1_REG

偏移地址 ：0x00B4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:00	RW	0	GENERAL_DBG1 General debug register 1 is used for storing flag or some data

2.3 存储空间映射（Memory Mapping）



2.4 存储控制器（Memory Controller）

2.4.1 概述

Memory Controller 兼容 Standard SPI /Dual SPI/Quad SPI/QPI(Quad Peripheral Interface)/PSRAM(SQPI)。

Memory Controller 通过 System bus 来进行 Flash 的擦除、读写 Flash/PSRAM、配置内部寄存器。通过 Code bus 读 Flash、读写 PSRAM。System bus 及 Code bus 都是 AHB 接口。SBUS 操作与 CBUS 操作不能同时发生。

Memory Controller 包含 SQPI Controller，支持对 SPI NOR FLASH 进行数据读写的操作控制，支持 16Mb SQPI PSRAM。

Memory Controller 的 IO 口包括：数据端口 IO0~IO3，CS_FLASH，CS_PSRAM。Flash 和 PSRAM 共用数据端口，通过 CS 片选，IO 电压必须一致，常见有 3.3V、1.8V。

主要特性如下：

- 支持 SPI 1/2/4 线模式收发
- 支持 SPI Mode0/1/2/3
- 支持 Flash 容量最大 2^32Bytes，常见有 64Mb，128Mb，256Mb
- 支持 CPU/DMA 通过系统总线对 Flash 的烧写和读取
- 支持 Flash XIP (Continuous Read)模式（进入/退出）
- 支持 Flash/PSRAM Wrap 模式（进入/退出）
- 支持常见 SPI 接口 Flash 的基本操作
- 支持 16Mb SQPI PSRAM
- 支持异常保护和异常中断
- 支持自动时钟切换

2.4.2 编程指引

以下为 Memory Controller 操作注意事项。

1. 合并 PSRAM SQPI(16M)和 FLASH，共用一个控制器，两路 CS，复用一路 IO0~IO3，支持 FLASH CBUS 读，PSRAM/FLASH CBUS 读/写，SBUS 读/写/发送命令；
2. SBUS 操作时，需要设置 C_RW_EN 为低电平，再拉高 START_SEND，否则触发 NOP 中断；
3. PSRAM SQPI 和 Flash 写共用 wr_buf 和 wr_fifo，SBUS 读共用 rd_buf 和 rd_fifo。意味着软件 SBUS 操作时，需要保证切换器件时候 FIFO 为空，否则可能造成错误。CBUS 的由硬件保证；
4. PSRAM CBUS 访问地址为：0x01400000-23FFFFF；Flash: 0x00400000 - 0x13FFFFF。通过 Flash or PSRAM Select 寄存器选择 SBUS 操作器件；
5. 支持 CBUS 单器件访问。设置寄存器 single_device_en 和 single_device_sel 进行单器件使能和器件选择，使能后两片地址区间都对 Flash 或 PSRAM 进行操作；
6. 0x00~0x08 为通用设置，同时对 Flash 和 PSRAM 生效。其他只对 Flash/PSRAM 生效的寄存器已在寄存器描述中标注；

7. CS 拉低时，进行切时钟。典型值：Flash 为 96MHz，PSRAM 为 133MHz。clk_sel_en 寄存器默认为 1，设成 0 则禁止切时钟，运行时钟一直为 flash 运行时钟；
8. XIP（Continuous Read Mode）只能用于 Flash，Read_Latency/Tcem 只用于 PSRAM；
9. PSRAM wrap 功能设置方法与 Flash 一致；
10. Flash 部分命令需要配置 read_dummy，write_dummy 作为扩展功能，暂不需要使用也不需要配置 read_latency；PSRAM 部分命令需要配置 read_latency，read_dummy 和 write_dummy 作为扩展功能，暂不需要使用；

2.4.3 Memory Controller 寄存器列表

模块名	基地址	
Memory Controller	0x4000B000	
寄存器名	**偏移地址**	**描述**
MEM_COM_CFG _REG	0x000	Memory Controller Common Configuration
SQPI_COM_CFG_REG	0x004	SQPI Controller Common Configuration
CACHE_CFG_REG	0x008	Cache Line Length Configuration
MEM_AC_CFG_REG	0x00C	Memory AC Character Timing Configuration
FLASH_C_READ_CFG_REG	0x010	Flash Code-bus Read Operation Configuration
FLASH_C_WRITE_CFG_REG	0x014	Flash Code-bus Write Operation Configuration
FLASH_C_RD_DUMMY_H_REG	0x018	Flash Code-bus Read Dummy Data Top Half
FLASH_C_RD_DUMMY_L_REG	0x01C	Flash Code-bus Read Dummy Data Bottom Half
FLASH_C_WR_DUMMY_H_REG	0x020	Flash Code-bus Write Dummy Data Top Half
FLASH_C_WR_DUMMY_L_REG	0x024	Flash Code-bus Write Dummy Data Bottom Half
FLASH_C_IO_SWIT_TIME_REG	0x028	FLASH Code-bus IO Switch Wait Time
S_RW_CFG_REG	0x02C	System-bus Read/Write Operation Configuration
S_ADDR_CFG_REG	0x030	System-bus Address Configuration
S_DUMMY_H_REG	0x034	System-bus Dummy Data Top Half
S_DUMMY_L_REG	0x038	System-bus Dummy Data Bottom Half
S_IO_SWIT_TIME_REG	0x03C	System-bus IO Switch Wait Time
S_WR_NUM_REG	0x040	System-bus Write Byte Number
S_RD_NUM_REG	0x044	System-bus Read Byte Number

START_SEND_REG	0x048	System-bus Start Send Register
FIFO_TRIG_LEV_REG	0x04C	FIFO Trigger Level
FIFO_STA_REG	0x050	FIFO Status Register
INT_EN_REG	0x054	Interrupt Enable Register
INT_STA_REG	0x058	Interrupt Status Register
FLASH_MOD_EXE_IND_REG	0x05C	XIP/WRAP Mode Executed Indication
START_ADDR0_REG	0x080	Address Field0 Start Position
END_ADDR0_REG	0x084	Address Field0 End Position
BIAS_ADDR0_REG	0x088	Address Field0 Bias
START_ADDR1_REG	0x090	Address Field1 Start Position
END_ADDR1_REG	0x094	Address Field1 End Position
BIAS_ADDR1_REG	0x098	Address Field1 Bias
START_ADDR2_REG	0x0A0	Address Field2 Start Position
END_ADDR2_REG	0x0A4	Address Field2 End Position
BIAS_ADDR2_REG	0x0A8	Address Field2 Bias
START_ADDR3_REG	0x0B0	Address Field3Start Position
END_ADDR3_REG	0x0B4	Address Field3 End Position
BIAS_ADDR3_REG	0x0B8	Address Field3 Bias
START_ADDR4 _REG	0x0C0	Address Field4 Start Position
END_ADDR4_REG	0x0C4	Address Field4 End Position
BIAS_ADDR4_REG	0x0C8	Address Field4 Bias
START_ADDR5_REG	0x0D0	Address Field5 Start Position
END_ADDR5_REG	0x0D4	Address Field5 End Position
BIAS_ADDR5_REG	0x0D8	Address Field5 Bias
S_WDATA_REG_REG	0x100	System-bus Write Data Register
S_RDATA_REG_REG	0x200	System-bus Read Data Register
PSRAM_COM_CFG_REG	0x800	PSRAM Common Configuration
PSRAM_CTRL_COM_CFG_REG	0x804	PSRAM Controller Common Configuration
PSRAM_CACHE_CFG_REG	0x808	PSRAM Cache Configuration

PSRAM_C_READ_CFG_REG	0x810	PSRAM Code-bus Read Operation Configuration
PSRAM_C_WRITE_CFG_REG	0x814	PSRAM Code-bus Write Operation Configuration
PSRAM_C_RD_DUMMY_H_REG	0x818	PSRAM Code-bus Read Dummy Data Top Half
PSRAM_C_RD_DUMMY_L_REG	0x81C	PSRAM Code-bus Read Dummy Data Bottom Half
PSRAM_C_WR_DUMMY_H_REG	0x820	PSRAM Code-bus Write Dummy Data Top Half
PSRAM_C_WR_DUMMY_L_REG	0x824	PSRAM Code-bus Write Dummy Data Bottom Half
PSRAM_C_IO_SWIT_TIME_REG	0x828	PSRAM Code-bus IO Switch Wait Time
PSRAM_FORCE_CFG_REG	0x86C	PSRAM Force Configure Register
PSRAM_COM_CFG_REG	0x870	PSRAM Common Configure Register

2.4.4 Memory Controller 寄存器描述

2.4.4.1 MEM_COM_CFG_REG

偏移地址 : 0x0000			**默认值: 0xB555_0082**
位置	**访问**	**默认值**	**描述**
31:30	RW	10	Flash Address Size Mode 00: Address Size 8bit. 01: Address Size 16bit. 10: Address Size 24bit. 11: Address Size 32bit.
29:28	RW	11	IO1 Port Vacancy Default Output Value. 00: Output 0. 01: Output 1. 1x: Output z. Note: IO1 Port Vacancy Output Value When Flash At Send State.
27:26	RW	01	IO2 Port Vacancy Default Output Value. 00: Output 0. 01: Output 1. 1x: Output z. Note: IO2 Port Vacancy Output Value When Flash At Send State.
25:24	RW	01	IO3 Port Vacancy Default Output Value. 00: Output 0.

			01: Output 1. 1x: Output z. Note: IO3 Port Vacancy Output Value When Flash At Send State.
23:16	/	/	
15:8	RW	0	System-bus HREADY Adjustable Wait Time Out Note:Default Value Indicates Wait Time Out Level =0xFFFF
7	RW	1	System-bus HREADY Time Out Enable 0: Disable 1: Enable
6	RW	0	Transfer FIFO Reset 0: Auto Clear to 0. 1: Reset Transfer FIFO. Note: Write '1' to this bit will reset the control portion of the transfer FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.
5	RW	0	Receiver FIFO Reset 0: Auto Clear to 0. 1: Reset Receiver FIFO. Note: Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.
4:3	/	/	/
2	RW	0	XIP(Continuous Read Mode) Mode Enable.(FLASH only) 0: Disable. 1: Enable. Note: Dummy Register Value Must Be Match When CPU Enable XIP Mode.
1	RW	1	XIP debug 0: When Flash CS Disable at Non-Data Period, XIP Mode Could not Exit By Itself. 1: When Flash CS Disable at Non-Data Period, XIP Mode Exit By Itself.
0	RW	0	Enable Code-bus Read/Write Operation. 0:Configuring Code-bus Read/Write Operation. 1:Configure Code-bus Over. Note1: When CPU exits Code-bus Read/Write Operation, Clear 0. Note2: When CPU Configure Code-bus Read/Write Operation Over , Set 1.

2.4.4.2 SQPI_COM_CFG_REG

偏移地址 ：0x0004			默认值: 0x0002_0000
位置	**访问**	**默认值**	**描述**
31:14	/	/	/
13:12	RW	0	Flash Wait Half Cycle Number Of Receive Data. 00: No Delay. 01: Delay 1 Half Cycle. 10: Delay 2 Half Cycle. 11: Delay 3 Half Cycle.
11:9	/	/	/
8	RW	0	Flash CS Polarity. 0: CS Signal is Low Enable. 1: CS Signal is High Enable.
7:5	/	/	/
4	RW	0	First Receive Bit Select. 0: MSB First 1: LSB First
3:2	/	/	/
1	RW	0	SPI Clock Polarity Control 0: Active High Polarity. 1: Active Low Polarity.
0	RW	0	SPI Clock/Data Phase Control 0: Phase 0(Leading Edge For Sample Data) 1: Phase 1(Leading Edge For Setup Data)

2.4.4.3 CACHE_CFG_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:14	/	/	/
13:12	RW	10	Write Cache Line Length Configuration 00: 8Bytes (64Bits) 01: 16Bytes (128Bits) 10: 32Bytes (256Bits) 11: 64Bytes (512Bits) It means write cache line length.
11:4	RW	0	Code-bus HREADY Adjustable Wait Time Out

			Note:Default Value Indicates Wait Time Out Level =0xFFFF
3	RW	1	Code-bus HREADY Time Out Enable 0: Disable 1: Enable
2	RW	1	Code-Bus Write Size Select 0: Code-Bus Write Request Size is Cache-line length 1: Code-Bus Write Request Size is Bus Size length(HSIZE) Note: SQPI Memory Controller Get Cache-line and Return Data Back to Bus At Same Time,So that SQPI Memory Controller Do not Care Whether Code-Bus Read Request From Cache or CPU
1:0	RW	1	Cache Line Length Configuration 00: 8Bytes (64Bits) 01: 16Bytes (128Bits) 10: 32Bytes (256Bits) Else: 16Bytes (128Bits) It means read cache line length.

2.4.4.4 MEM_AC_CFG_REG

偏移地址 : 0x000C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	RW	1	SPI Flash CS Enable Wait Cycle.(t_SLCH) Note: These Bits Stand For CS Active To Valid CLK Edge Setup Minimum Time.
23:16	RW	0	SPI Flash CS Disable Wait Cycle.(t_CHSH) Note: These Bits Stand For Valid CLK Edge To CS Active Hold Minimum Time.
15:8	RW	5	System-bus CS Deselect Wait Cycle(t_SHSL). Note1:These Bits Stand For The CS Deselect Minimum Time; Note2:Different Value from CS Deselect After Read/Write/Erase Note3:More Details in Data Sheet AC Characters: t_SHSL
7:0	RW	5	Code-bus CS Deselect Wait Cycle.(t_SHSL) Note1: When Select Flash,These Bits Stand For CS Minimum Deselect Time After Read. Note2: When Select PSRAM,Different Value from CS Deselect After Read/Write Note3:More Details in Data Sheet AC Characters: t_SHSL

2.4.4.5 FLASH_C_READ_CFG_REG

偏移地址 : 0x0010			**默认值: 0x0311_0001**
位置	**访问**	**默认值**	**描述**
31:24	RW	0x03	Read Command Send.

23	RW	0	Enable DMA read through I/D bus(flash/psram). 0: Disable. DMA read should through SBUS. 1: Enable.
22:20	RW	001	Bit Number Of Command Send Every Cycle. 000: No Send Command. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Command. Note1: Code-bus Command Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Command.
19	/	/	/
18:16	RW	001	Bit Number Of Address Send Every Cycle. 000: No Send Address. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Address. Note1: Code-bus Address Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Address. Note3: For Each Code-bus Operation, Send Address Is Necessary.
15	/	/	/
14:12	RW	0	Bit Number Of DUMMY Send Every Cycle. 000: No Send DUMMY . 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else: No Send DUMMY. Note1: Code-bus Dummy Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Dummy.
11	/	/	/
10:4	RW	0	DUMMY Data Bit Number. 0: Send 0 Bytes Dummy. 8: Send 1 Bytes Dummy. 16:Send 2 Bytes Dummy. ..... 64:Send 8 Bytes Dummy. Note1: Code-bus Send Dummy Bit Number Initial State is 0.

			Note2: Include XIP Mode Bits (M7-M0),WRAP Bits (W7-W0). Note3: Bit Number Value Must Be the Multiples of 8Bits, Max is 64 Bits. Note4: Same Command May Has Different Dummy Number At Different CLK Frequency, More Details See Data Sheet. Note5: If The Dummy Bit Number More Than 8 Bytes， Force to 8Bytes. Example：Dual Send Mode ：Dummy 4 clocks，Dummy Bits Number is 8
3	/	/	/
2:0	RW	1	Bit Number Of Data Get Every Cycle. 000: No Get Data. 001: Get 1 Bit Data Every Cycle. 010: Get 2 Bit Data Every Cycle. 011: Get 4 Bit Data Every Cycle. 100: Get 8 Bit Data Every Cycle. Else:No Get Data. Note1: Code-bus Get Read Data Mode Initial State is Single Mode. Note2: For Each Code-bus Operation, Get Data is Necessary.

2.4.4.6 FLASH_C_WRITE_CFG_REG

偏移地址 : 0x0014			**默认值: 0x0211_0001**
位置	**访问**	**默认值**	**描述**
31:24	RW	0x02	Write Command Send. Default is Normal Write
23	/	/	/
22:20	RW	1	Bit Number Of Command Send Every Cycle. 000: No Send Command. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Command. Note1: Code-bus Command Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Command.
19	/	/	/
18:16	RW	1	Bit Number Of Address Send Every Cycle. 000: No Send Address. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle.

			100: Send 8 Bit Data Every Cycle. Else:No Send Address. Note1: Code-bus Address Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Address. Note3: For Each Code-bus Operation, Send Address Is Necessary.
15	/	/	/
14:12	RW	0	Bit Number Of DUMMY Send Every Cycle. 000: No Send DUMMY. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else: No Send DUMMY. Note1: Code-bus Dummy Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Dummy.
11	/	/	/
10:4	RW	0	DUMMY Data Bit Number. 0: Send 0 Bytes Dummy. 8: Send 1 Bytes Dummy. 16:Send 2 Bytes Dummy. ..... 64:Send 8 Bytes Dummy. Note1: Code-bus Send Dummy Bit Number Initial State is 0. Note2: Bit Number Value Must Be the Multiples of 8Bits, Max is 64 Bits. Note3: Same Command May Has Different Dummy Number At Different CLK Frequency, More Details See Data Sheet. Note4: If The Dummy Bit Number More Than 8 Bytes， Force to 8 Bytes. Example：Dual Send Mode ：Dummy 4 clocks，Dummy Bits Number is 8
3	/	/	/
2:0	RW	1	Bit Number Of Data Send Every Cycle. 000: No Send Data. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Data. Note1: Code-bus Send Data Mode Initial State is Single Mode. Note2: For Each Code-bus Operation, Get Data is Necessary.

2.4.4.7 FLASH_C_RD_DUMMY_H_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Top Half 32bits Of Code-bus DUMMY Data.

2.4.4.8 FLASH_C_RD_DUMMY_L_REG

偏移地址 ：0x001C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Bottom Half 32bits Of Code-bus DUMMY Data.

2.4.4.9 FLASH_C_WR_DUMMY_H_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Top Half 32bits Of Code-bus DUMMY Data.

2.4.4.10 FLASH_C_WR_DUMMY_L_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Bottom Half 32bits Of Code-bus DUMMY Data.

2.4.4.11 FLASH_C_IO_SWIT_TIME_REG

偏移地址 ：0x0028			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	/	/	When the OPI Port Exist I/O Switch, Port Trans/Get Data Needs Suspend.

2.4.4.12 S_RW_CFG_REG

偏移地址 ：0x002C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:23	/	/	/
22:20	RW	0	Bit Number Of Command Send Every Cycle. 000: No Send Command. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle.

			100: Send 8 Bit Data Every Cycle. Else:No Send Command. Note: These Bits Indicate Whether Or Not Send Command.
19	/	/	/
18:16	RW	0	Bit Number Of Address Send Every Cycle. 000: No Send Address. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Address. Note: These Bits Indicate Whether Or Not Send Address.
15	/	/	/
14:12	RW	0	Bit Number Of DUMMY Send Every Cycle. 000: No Send DUMMY. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else: No Send DUMMY. Note: These Bits Indicate Whether Or Not Send Dummy.
11	/	/	/
10:4	RW	0	DUMMY Data Bit Number. 0: Send 0 Bytes Dummy. 8: Send 1 Bytes Dummy. 16:Send 2 Bytes Dummy. ..... 64:Send 8 Bytes Dummy. Note1:System-bus Send Dummy Bit Number Initial State is 0. Note2: Bit Number Value Must Be the Multiples of 8Bits, Max is 64 Bits. Note3: Same Command May Has Different Dummy Number At Different CLK Frequency, More Details See Data Sheet. Note4: If The Dummy Bit Number More Than 8 Bytes， Force to 8 Bytes. Example：Dual Send Mode ：Dummy 4 clocks，Dummy Bits Number is 8
3	/	/	/
2:0	RW	0	Bit Number Of System-bus Data Get/Write Every Cycle. 000: Neither Get Nor Send Data Operation. 001: Get/Send 1 Bit Data Every Cycle.

			010: Get/Send 2 Bit Data Every Cycle. 011: Get/Send 4 Bit Data Every Cycle. 100: Get/Send 8 Bit Data Every Cycle. Else:Neither Get Nor Send Data Operation. Note1: These Bits Indicate Wether Or Not Send/Get Data. Note2: Work With Write/Read Number To Indicate Current Operation is Send or Get Data State As Long As These Bits Are Non-Zero.

2.4.4.13 S_ADDR_CFG_REG

偏移地址 : 0x0030			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	32 Bits Flash Page Address Of System-bus Operation. Note:If the Flash Address Size is 24 bits， Write Low 24 Bits.

2.4.4.14 S_DUMMY_H_REG

偏移地址 : 0x0034			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	Top Half 32bits Of Dummy Data.

2.4.4.15 S_DUMMY_L_REG

偏移地址 : 0x0038			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	Bottom Half 32bits Of Dummy Data.

2.4.4.16 S_IO_SWIT_TIME_REG

偏移地址 : 0x003C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	RW	0	System-bus Read Latency Wait Cycle
23:0	/	/	/

2.4.4.17 S_WR_NUM_REG

偏移地址 : 0x0040			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	WC	0	System-bus Write Number(Byte) 0:Non-Write. 1:Write 1 Byte. 2:Write 2 Bytes.

			3:Write 3 Bytes. ..... Note1: These Bits Indicate Current Operation is Write Data To Flash. Note2: If CPU Execute Write Data Operation, Bit Number Of System-bus Data Get/Write Every Cycle Must Be Configure Non-Zero Value. Note3: If Select Flash,Then CPU Wants Program More Than 256 Bytes Data , Divide Multiple Pages to Program， Every Time CPU Execute Page Program, Needs Check the Flash BUSY Bit.

2.4.4.18 S_RD_NUM_REG

偏移地址 : 0x0044			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	WC	0	System-bus Read Number(Byte) 0:Non-Read. 1:Read 1 Byte. 2:Read 2 Bytes. 3:Read 3 Bytes. ..... Note1: These Bits Indicate Current Operation is Read Data From Flash. Note2: If CPU Execute Read Data Operation, Bit Number Of System-bus Data Get/Write Every Cycle Must Be Configure Non-Zero Value.

2.4.4.19 START_SEND_REG_REG

偏移地址 : 0x0048			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	WC	0	Enable System-bus Operation 0: System-bus Operation is Configuring. 1: System-bus Operation Configure Over. Note1: If System-bus is Configuring Write Operation, This Bit should be Configured after all the Register Which Write Operation Needs Complete Configuration and Before Writing Data to Write FIFO. Note2: If System-bus is Configuring Read Operation, This Bit should be Configured after all the Register Which Read Operation Needs Complete Configuration and Before Reading Data From Read FIFO. Note3: If This Bit Current Value is 1, Wait Memory Controller Clear to 0, CPU Could Configure Next System-bus Operation.

2.4.4.20 FIFO_TRIG_LEV_REG

偏移地址 ：0x004C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	RW	0x6F	Write FIFO Full Request Trigger Level(Byte).
23:16	RW	0x0F	Write FIFO Empty Request Trigger Level(Byte).
15:8	RW	0x6F	Read FIFO Full Request Trigger Level(Byte).
7:0	RW	0x0F	Read FIFO Empty Request Trigger Level(Byte).

2.4.4.21 FIFO_STA_REG_REG

偏移地址 ：0x0050			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	/
25	R	0	Read Buffer Full Flag.
24	R	0	Write Buffer Full Flag.
23	R	0	Write Buffer Could or Not Write.
22:20	R	0	Write Buffer Counter(Byte) These Bits Indicate Number of Bytes in Write Buffer.
19	R	0	Read Buffer Could or Not Read
18:16	R	0	Read Buffer Counter(Byte) These Bits Indicate Number of Bytes in Read Buffer.
15:8	R	0	Write FIFO Counter(Byte) These Bits Indicate Number of Bytes in Write FIFO. 0: 0 Byte in Write FIFO. 1: 1 Bytes in Write FIFO. … 128: 128 Bytes in Write FIFO.
7:0	R	0	Read FIFO Counter(Byte) These Bits Indicate Number of Bytes in Read FIFO. 0: 0 Byte in Read FIFO. 1: 1 Byte in Read FIFO. … 128: 128 Bytes in Read FIFO.

2.4.4.22 INT_EN_REG_REG

偏移地址 ：0x0054			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15	RW	0	When DMA write address was not in the non-cacheable field which were configured in the DCACHE register mr010~mr034, send interrupt to CPU. 0: Disable. 1: Enable.
14	RW	0	PSRAM read latency Time Out Interrupt Enable 0:Disable. 1:Enable.
13	RW	0	System-bus HREADY Time Out Interrupt Enable 0:Disable. 1:Enable.
12	RW	0	Transfer Completed Interrupt Enable 0: Disable. 1: Enable.
11	RW	0	Write FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
10	RW	0	Write FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
9	RW	0	Read FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
8	RW	0	Read FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
7	/	/	/
6	RW	0	Write FIFO Full Interrupt Enable 0: Disable. 1: Enable.
5	RW	0	Write FIFO Empty Interrupt Enable 0: Disable. 1: Enable.
4	RW	0	Write FIFO Ready Request Interrupt Enable

			0: Disable. 1: Enable.
3	/	/	/
2	RW	0	Read FIFO Full Interrupt Enable 0: Disable. 1: Enable.
1	RW	0	Read FIFO Empty Interrupt Enable 0: Disable. 1: Enable.
0	RW	0	Read FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.

2.4.4.23 INT_STA_REG_REG

偏移地址 : 0x0058			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:14	/	/	/
13	W1C/R	0	System-bus HREADY Time Out Interrupt Flag 0:System-bus HREADY Time Out Not Happens. 1: System-bus HREADY Time Out Happens.
12	W1C/R	0	Transfer Completed Interrupt Flag 0: Busy. 1: Transfer Completed.
11	W1C/R	0	Write FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing “1” to this bit clears it.
10	W1C/R	0	Write FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing “1” to this bit clears it.
9	W1C/R	0	Read FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing “1” to this bit clears it.
8	W1C/R	0	Read FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing “1” to this bit clears it.
7	/	/	/
6	W1C/R	0	Write FIFO Full Interrupt Flag 0: Write FIFO is Not Full.

			1: Write FIFO is Full. Note: This bit is set when the Write FIFO is full. Writing “1” to this bit clears it.
5	W1C/R	0	Write FIFO Empty Request Interrupt Flag 0: Write FIFO always contains one or more bytes. 1: Write FIFO has been empty. Note: This bit is set if the Write FIFO is empty. Writing “1” to this bit clears it.
4	W1C/R	0	Write FIFO Empty Request Interrupt Flag 0: WF_WL > WF_TRIG_LEVEL. 1: WF_WL <= WF_TRIG_LEVEL has happened. Note: This bit is set any time if WF_WL <= WF_TRIG_LEVEL. Writing “1” to this bit clears it. Where WF_WL is the water level of Write FIFO.
3	/	/	/
2	W1C/R	0	Read FIFO Full Interrupt Flag 0: Not Full. 1: Read FIFO has been Full. Note: This bit is set when Read FIFO is full(>= full_trigger_level). Writing “1” to this bit clears it.
1	W1C/R	0	Read FIFO Empty Interrupt Flag 0: Not Empty. 1: Read FIFO has been Empty. Note: This bit is set if the Read FIFO is empty. Writing “1” to this bit clears it.
0	W1C/R	0	Read FIFO Ready Request Interrupt Flag 0: RF_WL < RX_TRIG_LEVEL. 1: RF_WL >= RX_TRIG_LEVEL has happened. This bit is set any time if RF_WL >= RF_TRIG_LEVEL. Writing “1” to this bit clears it. Where RF_WL is the water level of Read FIFO.

2.4.4.24 FLASH_MOD_EXE_IND_REG

偏移地址 : 0x005C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	R	0	flash WRAP Psram wrap is always working, so it does not need flag. 0:Wrap Mode Has Not Taken Effect in Memory. 1:Wrap Mode Has Taken Effect in Memory.
0	R	0	FLASH ONLY

			0: XIP Mode Has Not Taken Effect in Memory. 1: XIP Mode Has Taken Effect in Memory

2.4.4.25 START_ADDR0_REG

偏移地址 : 0x0080			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field0 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.26 END_ADDR0_REG

偏移地址 : 0x0084			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field0 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.27 BIAS_ADDR0_REG

偏移地址 : 0x0088			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	RW	0	Address Field0 Bias Enable 1: Bias Enabled, add bias when address is between Address Field0 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field0 Bias

2.4.4.28 START_ADDR1_REG

偏移地址 : 0x0090			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field1 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.29 END_ADDR1_REG

偏移地址 ：0x0094			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field1 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.30 BIAS_ADDR1_REG

偏移地址 ：0x0098			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0	Address Field1 Bias Enable 1: Bias Enabled, add bias when address is between Address Field1 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field1 Bias

2.4.4.31 START_ADDR2_REG

偏移地址 ：0x00A0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field2 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.32 END_ADDR2_REG

偏移地址 ：0x00A4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field2 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.33 BIAS_ADDR2_REG

偏移地址 ：0x00A8			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0	Address Field2 Bias Enable 1: Bias Enabled, add bias when address is between Address Field2 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field2 Bias

2.4.4.34 START_ADDR3_REG

偏移地址 ：0x00B0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field3 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.35 END_ADDR3_REG

偏移地址 ：0x00B4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field3 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.36 BIAS_ADDR3_REG

偏移地址 ：0x00B8			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0	Address Field3 Bias Enable 1: Bias Enabled, add bias when address is between Address Field3 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field3 Bias

2.4.4.37 START_ADDR4_REG

偏移地址 ：0x00C0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field4 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.38 END_ADDR4_REG

偏移地址 ：0x00C4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field4 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.39 BIAS_ADDR4_REG

偏移地址 ：0x00C8			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0	Address Field4 Bias Enable 1: Bias Enabled, add bias when address is between Address Field4 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field4 Bias

2.4.4.40 START_ADDR5_REG

偏移地址 ：0x00D0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:26	/	/	
25:4	RW	0	Address Field5 Start Position Note: With unit of 16B
3:0	/	/	/

2.4.4.41 END_ADDR5_REG

偏移地址 ：0x00D4			默认值: 0x0000_0000
位置	访问	默认值	描述
31:26	/	/	
25:4	RW	0	Address Field5 End Position Note: With unit of 16B
3:0	/	/	/

2.4.4.42 BIAS_ADDR5_REG

偏移地址 ：0x00D8			默认值: 0x0000_0000
位置	访问	默认值	描述
31	RW	0	Address Field5 Bias Enable 1: Bias Enabled, add bias when address is between Address Field5 Start Position and End Position. 0: Bias Disabled.
30:0	RW	0	Address Field5 Bias

2.4.4.43 S_WDATA_REG

偏移地址 ：0x0100			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	System-bus Write Data Register. Note: Write FIFO Entrance.

2.4.4.44 S_RDATA_REG

偏移地址 ：0x0200			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R	0	System-bus Read Data Register. Note: Read FIFO Exit.

2.4.4.45 PSRAM_ COM_CFG_REG

偏移地址 ：0x0800			默认值: 0x0000_0000
位置	访问	默认值	描述
31:30	RW	10	Psram Address Size Mode 00: Address Size 8bit. 01: Address Size 16bit. 10: Address Size 24bit.

			11: Address Size 32bit.
[29:0]	/	/	/

2.4.4.46 PSRAM_CTRL_COM_CFG_REG

偏移地址 : 0x0804			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:17	/	/	/
16	RW	0	When DMA write address was not in the non-cacheable field which were configured in the DCACHE register mr010~mr034, the write operation should not take into effect. 0: write operation still take into effect. 1: write oper ation would not take into effect.
15:0	/	/	/

2.4.4.47 PSRAM_CACHE_CFG_REG

偏移地址 : 0x0808			**默认值: 0x0000_8000**
位置	**访问**	**默认值**	**描述**
31	RW	0	Auto send data when not meet cache line length but timeout. Used with bit[30:17]. For example, when cache line length is 128bits, after receive address 0x0, 0x4, 0x8 from upstream, controller didn’ t get address 0xC data for a long time, then send 0x0, 0x4, 0x8 when this register configured 1.
30:16	RW	0	Wait Cache Line data timeout cycle.
15	RW	1	Auto cut sequential word send into two write operation when address cross page boundary. PSRAM cbus write only! For SQPI 16Mb, page size is 512Byte. Page size is configured in 0x870.
14:0	/	/	/

2.4.4.48 PSRAM_C_READ_CFG_REG

偏移地址 : 0x0810			**默认值: 0x0311_0001**
位置	**访问**	**默认值**	**描述**
31:24	RW	0x03	Read Command Send.
23	/	/	/
22:20	RW	001	Bit Number Of Command Send Every Cycle. 000: No Send Command. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle.

			011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Command. Note1: Code-bus Command Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Command.
19	/	/	/
18:16	RW	001	Bit Number Of Address Send Every Cycle. 000: No Send Address. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Address. Note1: Code-bus Address Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Address. Note3: For Each Code-bus Operation, Send Address Is Necessary.
15	/	/	/
14:12	RW	0	Bit Number Of DUMMY Send Every Cycle. 000: No Send DUMMY . 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else: No Send DUMMY. Note1: Code-bus Dummy Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Dummy.
11	/	/	/
10:4	RW	0	DUMMY Data Bit Number. 0: Send 0 Bytes Dummy. 8: Send 1 Bytes Dummy. 16:Send 2 Bytes Dummy. ..... 64:Send 8 Bytes Dummy. Note1: Code-bus Send Dummy Bit Number Initial State is 0. Note2: Include XIP Mode Bits (M7-M0),WRAP Bits (W7-W0). Note3: Bit Number Value Must Be the Multiples of 8Bits, Max is 64 Bits. Note4: Same Command May Has Different Dummy Number At Different CLK Frequency, More Details See Data Sheet. Note5: If The Dummy Bit Number More Than 8 Bytes， Force to 8Bytes. Example：Dual Send Mode ：Dummy 4 clocks，Dummy Bits Number

			is 8
3	/	/	/
2:0	RW	1	Bit Number Of Data Get Every Cycle. 000: No Get Data. 001: Get 1 Bit Data Every Cycle. 010: Get 2 Bit Data Every Cycle. 011: Get 4 Bit Data Every Cycle. 100: Get 8 Bit Data Every Cycle. Else:No Get Data. Note1: Code-bus Get Read Data Mode Initial State is Single Mode. Note2: For Each Code-bus Operation, Get Data is Necessary.

2.4.4.49 PSRAM_C_WRITE_CFG_REG

偏移地址 ：0x0814			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	RW	0x02	Write Command Send. Default is Normal Write
23	/	/	/
22:20	RW	1	Bit Number Of Command Send Every Cycle. 000: No Send Command. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Command. Note1: Code-bus Command Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Command.
19	/	/	/
18:16	RW	1	Bit Number Of Address Send Every Cycle. 000: No Send Address. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Address. Note1: Code-bus Address Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Address. Note3: For Each Code-bus Operation, Send Address Is Necessary.
15	/	/	/
14:12	RW	0	Bit Number Of DUMMY Send Every Cycle.

			000: No Send DUMMY. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else: No Send DUMMY. Note1: Code-bus Dummy Send Mode Initial State is Single Mode. Note2: These Bits Indicate Whether Or Not Send Dummy.
11	/	/	/
10:4	RW	0	DUMMY Data Bit Number. 0: Send 0 Bytes Dummy. 8: Send 1 Bytes Dummy. 16:Send 2 Bytes Dummy. ..... 64:Send 8 Bytes Dummy. Note1: Code-bus Send Dummy Bit Number Initial State is 0. Note2: Bit Number Value Must Be the Multiples of 8Bits, Max is 64 Bits. Note3: Same Command May Has Different Dummy Number At Different CLK Frequency, More Details See Data Sheet. Note4: If The Dummy Bit Number More Than 8 Bytes， Force to 8 Bytes. Example：Dual Send Mode ：Dummy 4 clocks，Dummy Bits Number is 8
3	/	/	/
2:0	RW	1	Bit Number Of Data Send Every Cycle. 000: No Send Data. 001: Send 1 Bit Data Every Cycle. 010: Send 2 Bit Data Every Cycle. 011: Send 4 Bit Data Every Cycle. 100: Send 8 Bit Data Every Cycle. Else:No Send Data. Note1: Code-bus Send Data Mode Initial State is Single Mode. Note2: For Each Code-bus Operation, Get Data is Necessary.

2.4.4.50 PSRAM_C_RD_DUMMY_H_REG

偏移地址 : 0x0818			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	Top Half 32bits Of Code-bus DUMMY Data.

2.4.4.51 PSRAM_C_RD_DUMMY_L_REG

偏移地址 ：0x081C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Bottom Half 32bits Of Code-bus DUMMY Data.

2.4.4.52 PSRAM_C_WR_DUMMY_H_REG

偏移地址 ：0x0820			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Top Half 32bits Of Code-bus DUMMY Data.

2.4.4.53 PSRAM_C_WR_DUMMY_L_REG

偏移地址 ：0x0824			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	Bottom Half 32bits Of Code-bus DUMMY Data.

2.4.4.54 PSRAM_C_IO_SWIT_TIME_REG

偏移地址 ：0x0828			默认值: 0x0000_0000
位置	访问	默认值	描述
31:24	RW	0	PSRAM Code-bus Read Latency Wait Cycle
23:0	RW	/	/
NOTE When the OPI Port Exist I/O Switch, Port Trans/Get Data Needs Suspend.			

2.4.4.55 PSRAM_FORCE_CFG_REG

偏移地址 ：0x086C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:2	/	/	
1:0	RW	0x0	Psram Wait Half Cycle Number Of Receive Data. 00: No Delay. 01: Delay 1 Half Cycle. 10: Delay 2 Half Cycle. 11: Delay 3 Half Cycle.

2.4.4.56 PSRAM_COM_CFG_REG

偏移地址 ：0x0870			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:28	/	/	/
27:16	RW	0x1C0	Maximum CE# low cycle number. CE# should not be kept low for more than 4 us. This value is different for various frequency, default value is for working in 133MHz. When configured 0, it means not checking CE# low width.
15	/	/	
14	RW	1’ b0	Write or read could start on random address. 0: Write or read should start on even address. 1: Write or read could start on odd or even address. When write or read mode registers, configure this to 1. When memory access, configure 0.
13:0	/	/	/

3 时钟和复位

3.1 全局电源、复位、时钟管理（GPRCM）

3.1.1 概述

GPRCM 模块管理整个系统的电源、复位和时钟，工作在 AO（always on）电源域。关于 XR806 电源架构、上下电时序、时钟描述等信息可参考《XR806 Datasheet》。

注意

GPRCM 相关寄存器被放置在 RTC 电源域，以保证在关断内部 LDO 或 DCDC 使系统掉电时，这些寄存器的值可以保持不变。当检测到 GPIO 或电源等外部中断事件时，系统可以自动启动，并能正确读取这些寄存器的值。

3.1.2 GPRCM 寄存器列表

模块名	基地址	
Power, Reset and Clock Manager	0x40040000/0xA0040000	
寄存器名	**偏移地址**	**描述**
SYS_TOP_LDO _SMPS_CTRL_REG	0x0000	System TOP_LDO&SMPS Control Register
SYS_EXT_LDO_DIG_LDO_SW_CTRL_REG	0x0004	System EXT_LDO&DIG_LDO & Switch Control Register
SYS_LFCLK_CTRL_REG	0x0008	System Low Frequency Clock Control
SYS_HOSC_TYPE_REG	0x000C	System HOSC Type
SYS_RCOSC_CAL_CTRL_REG	0x0010	System RC-OSC Calibration Control
SYS_PLL_CTRL_REG	0x0020	System PLL Control
SYS_CLK1_CTRL_REG	0x0024	System Clock 1 Control
SYS_CLK3_CTRL_REG	0x002C	System Clock 3 Control
DEV_CLK_CTRL_REG	0x0034	Device Clock Control
DCXO_CTRL_REG	0x0058	DCXO control
CONN_BOOT_FLAG_REG	0x0070	Connect mode flag
POWERCTRL_CFG_REG	0x0074	Power control configuration register
SYS1_CTRL_REG	0x080	System 1 Control
SYS1_STATUS_REG	0x084	System 1 Status
SYS2_CTRL_REG	0x088	System 2 Control

SYS2_STATUS_REG	0x08C	System 2 Status
SYS3_CTRL_REG	0x090	System 3 Control
SYS3_STATUS_REG	0x094	System 3 Status
SYS1_WAKEUP_CTRL_REG	0x098	System 1 wakeup control
SYS2_WAKEUP_CTRL_REG	0x09C	System 2 wakeup control
SYS1_SLEEP_CTRL_REG	0x0A0	System 1 Sleep control
SYS2_SLEEP_CTRL_REG	0x0A4	System 2 Sleep control
DCXO_STABLE_REF_TIME_REG	0x0A8	DCXO Stable Reference Time
DPLL_STABLE_REF_TIME_REG	0x0AC	DPLL Stable Reference Time
LDO_STABLE_REF_TIME_REG	0x0B0	LDO Stable Reference Time
DIGITAL_SWITCH_REF_TIME_REG	0x0B4	Digital Switch Reference Time
SRAM_VOL_CTRL_REG	0x0B8	SRAM Voltage Control
BANDGAP_STABLE_REF_TIME_REG	0x0BC	Band Gap Stable Reference Time
DCDC_STABLE_REF_TIME_REG	0x0C0	DCDC Stable Reference Time
BLE_RTC_RST_CTRL_REG	0x0D0	BLE RTC Reset control Register
RFAS_CTRL_REG	0x0D8	RFAS Reset control Register
AR400A_BOOT_FLAG_REG	0x0100	AR400A boot flag
AR400A_BOOT_ADDR_REG	0x0104	AR400A boot address
AR400A_BOOT_ARG_REG	0x0108	AR400A boot argument
AR400N_PRIV_REG0	0x010C	AR400A Private Register
AR400N_PRIV_REG1	0x0110	AR400A Private Register
AR400N_PRIV_REG2	0x0114	AR400A Private Register
AR400A_PRIV_REG3	0x0118	AR400A Private Register
AR400A_PRIV_REG4	0x011c	AR400A Private Register
AR400A_WAKE_TIMER_CNT_REG	0x0120	AR400A wakeup timer counter
AR400A_WAKE_TIMER_CTRL_REG	0x0124	AR400A wakeup timer control
AR400A_PRIV_REG5	0x0128	AR400A Private Register
AR400A_PRIV_REG6	0x012c	AR400A Private Register
AR400A_IO_WAKE_EN_REG	0x0130	AR400A IO Wakeup Enable
AR400A_IO_WAKE_DEB_CLK_REG	0x0134	AR400A IO Wakeup debounce clock

AR400A_IO_WAKE_ST_REG	0x0138	AR400A IO Wakeup Status
AR400A_IO_HOLD_CTRL_REG	0x013c	AR400A IO Hold Control
AR400A_IO_WUP_GEN_REG	0x0140	AR400A IO Wakeup Global Enable
AR400A_IO_WAKE_DEB_CYCLES0_REG	0x0144	AR400A IO Wakeup debouce clock cycles 0
AR400A_IO_WAKE_DEB_CYCLES1_REG	0x0148	AR400A IO Wakeup debouce clock cycles 1
LDO_MODE_SW_SEL_REG	0x0150	LDO Mode Software Select
DCDC_PARAM_REG	0x0200	DCDC Parameter Register
ANA_BANDGAP_REG	0x0204	ANA Bandgap Control Register
CLK_LDO_PARAM_REG	0x0208	Clock LDO Parameter Register
DIG_LDO_PARAM_REG	0x020C	Digital LDO Parameter Register
DPLL_ST_REG	0x0210	DPLL Status Register
CFG_IO_STATUS_REG	0x214	Config IO Status
CPU_RST_SRC_REG	0x218	CPU reset source register
WLAN_HIF_OV_CTRL_REG	0x21c	WLAN HIF override control register
SRAM_BIST_CFG_REG	0x220	SRAM configure register
WLAN_SRAM_SHARE_REG	0x224	WLAN SRAM share control register
BLE_SRAM_SHARE_CTRL_REG	0x228	BLE 16K SRAM share control register
LPUART0_WAKEUP_CTRL_REG	0x230	LPUART0 wakeup control register
LPUART1_WAKEUP_CTRL_REG	0x234	LPUART1 wakeup control register
GPADC_CLK_CTRL_REG	0x238	GPADC core clock control register
CAPSEN_CLK_CTRL_REG	0x23C	CAPSEN core clock control register
WKUP_SRC_BUS_CLK_CTRL_REG	0x240	Wakeup source bus clock control register
WKUP_SRC_RST_CTRL_REG	0x244	Wakeup source reset control register
FLASH_ENCRYPT_AES_NONCE0_REG	0x250	Flash encrypt module AES nonce low bits register
FLASH_ENCRYPT_AES_NONCE1_REG	0x254	Flash encrypt module AES nonce high bits register
BLE_RCOSC_CALIB_REG0	0x260	RCOSC calibration control register0
BLE_RCOSC_CALIB_REG1	0x264	RCOSC calibration control register1
BLE_CLK32K_SWITCH_REG0	0x268	Clock 32k auto switch register0
BLE_CLK32K_SWITCH_REG1	0x26c	Clock 32k auto switch register1

3.1.3 GPRCM 寄存器描述

3.1.3.1 SYS_TOP_LDO _SMPS_CTRL_REG

偏移地址 ：0x0000			默认值: 0x0F00_8000
位置	**访问**	**默认值**	**描述**
31:29	/	/	/
28:25	R/W	0x7	TOP_LDO_VOLTAGE_SEL Lower power top ldo voltage select N: 0~15 0: 0.9V 1: 1.0V 2: 1.1V 3: 1.2V 4: 1.3V 5: 1.4V 6: 1.5V 7: 1.6V 8: 1.7V 9: 1.8V 10: 1.9V 11: 2.0V 12: 2.1V 13: 2.2V 14: 2.3V 15: 2.4V the default is 1600mV Note: This bit will only be reset to the default value in power-on-reset operation. When the system is waked up from the deep sleep mode by some external events, this bit will keep the value which is set by the last write operation.
24	R/W	0x1	TOP_LDO_EN Lower power top ldo enable 0: enable 1: disable
23:16	/	/	/
15:12	R/W	0x8	SMPS_VOLTAGE_SEL 1.0V – 2.5V) SMPS(DC-DC) voltage select N: 0~15 0: 1.0V 1: 1.1V 2: 1.2V

			3: 1.3V 4: 1.4V 5: 1.5V 6: 1.6V 7: 1.7V 8: 1.8V 9: 1.9V 10: 2.0V 11: 2.1V 12: 2.2V 13: 2.3V 14: 2.4V 15: 2.5V the default is 1800mV Note: This bit will only be reset to the default value in power-on-reset operation. When the system is waked up from the deep sleep mode by some external events, this bit will keep the value which is set by the last write operation.
11:10	/	/	/
9	RW	0	DIGLDO_OFF_SMPS_ON 0:When DIG_LDO was turned off, SMPS could turned off either. 1: When DIG_LDO was turned off, SMPS remain turned on
8	RW	0	SYS_STANDBY_SMPS_OFF 0: When system was in standby mode, SMPS could remain turned on 1: When system was in standby mode, SMPS should turned off
7	RW	0	SMPS_PWM_SEL_EN Enable SMPS_PWM_SEL function.
6：4	RW	0	SMPS_PWM_SEL SMPS_PWM could from the following source: 000：clk_RfipDpllStart 001：clk_RfipDcxoStart 010：WLAN PHY enable 011：APP CPU enable 100：WLAN CPU enable others：BLE RF enable
3	/	/	
2	RW	0	OVR_SMPS_DETCT Overwirte SMPS_DETECT by software.
1	RW	0	OVR_SMPS_DETCT_VALUE

			Overwrite value of SMPS_DETECT
0	R		SMPS_DETECT SMPS detect value from powerctrl

3.1.3.2 SYS_EXT_LDO_DIG_LDO_SW_CTRL_REG

偏移地址 ：0x0004			**默认值: 0x0002_0103**
位置	**访问**	**默认值**	**描述**
31:28	/	/	/
27:24	R/W	0	DIG_LDO_RET_VOL_SEL LDO1 retention voltage select 0 ~ 12: N 0: 1125mV 1: 1025mV 2: 925mV 3: 825mV 4: 725mV 5: 625mV 8: 1175mV 9: 1225mV 10: 1275mV 11: 1325mV 12: 1375mV others: reserved *the default is 1125mV*
23	R/W	0x0	*EXT_LDO_BYPASS* 0: EXT_LDO not be bypassed 1: EXT_LDO be bypassed
22:21	R/W	0x0	EXT_LDO_SW_TRIM Bit[1:0], option select of the regulate cycle when EXT_LDO in switch mode
20	R/W	0x0	EXT_LDO_SW_MODE 0: EXT_LDO not enter switch mode 1: EXT_LDO enter switch mode
19:18	R/W	0x0	EXT_LDO_VOL_SEL EXT_LDO voltage select 0: 3.3V 1: 3.1V

			2: 2.8V 3: 2.5V *the default is 3.3V*
17:16	R/W	0x2	EXT_LDO_MODE EXT_LDO mode 00: always off 01: on/off same as TOP_LDO 1x: always on
15	/	/	/
14	R	0	SW5_STATUS WLAN System Power Switch SW5 status 1: SW5 is on 0: SW5 is off
13:9	/	/	/
8	R	1	SW1_STATUS AR400A and Application System Power Switch status 1: SW1 is on 0: SW1 is off *Note: this bit will only be set by **POWERCTRL** module.*
7:4	R/W	0	DIG_LDO_VOL_SEL 0 ~ 12: N 0: 1125mV 1: 1025mV 2: 925mV 3: 825mV 4: 725mV 5: 625mV 8: 1175mV 9: 1225mV 10: 1275mV 11: 1325mV 12: 1375mV others: reserved *the default is 1125mV*
3:2	/	/	/
1	R/W	1	PLL_LDO_EN

			1: Write 1 to enable the PLL_LDO_EN. 0: write 0 to disable the PLL_LDO_EN.
0	R	1	DIG_LDO_EN 1: Write 1 to enable the LDO1. 0: write 0 to disable the LDO1. Note: this bit will only be set by POWERCTRL module.

3.1.3.3 SYS_LFCLK_CTRL_REG

偏移地址 : 0x0008			**默认值: 0xC100_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	1	OSC32K_EN 1: enable the 32768 Oscillator 0: disable the 32768 Oscillator
30	R/W	1	RC32K_EN 1: enable the 32768 RC Oscillator 0: disable the 32768 RC Oscillator
29:25	/	/	/
24	R/W	1	LFCLK_SRC_SEL Low frequency clock source select 0: source the LFCLK from the internal 32768 RC oscillator 1: source the LFCLK from the external 32768 crystal oscillator
23:8	R/W	0	PAD_CLOCK_OUT_FACTOR_M factor M, M= Factor + 1 Output clock frequency Fout = Fsrc/M
2:1	R/W	0	PAD_CLOCK_OUT_SEL GPIO PAD 32KOSCO clock source select 0: source the LFCLK from the internal 32768 RC oscillator 1: source the LFCLK from the BLE 32K 2: source the RCO_CALIB 32K 3: source the HFCLK from the external crystal oscillator
0	R/W	0	PAD_CLOCK_OUT_EN GPIO PAD 32KOSCO clock output enable.

			0: disable 1: enable

3.1.3.4 SYS_HOSC_TYPE_REG

偏移地址 : 0x000C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1:0	R/W	0	HOSC_TYPE 0: System uses 26MHz HOSC 1: System uses 40MHz HOSC 2: System uses 24MHz HOSC 3: System uses 32MHz HOSC *Note: This bit is set by application software and must be consistent with the real situation. A wrong configuration will cause the RCOSC calibration fail.*

3.1.3.5 SYS_RCOSC_CAL_CTRL_REG

偏移地址 : 0x0010			默认值: 0x000C_8001
位置	**访问**	**默认值**	**描述**
31:28	/	/	/
27:8	R	0xc80	RC-OSC Frequency V=FREQ/10
7:1	/	/	/
0	R/W	1	RC-OSC Calibration Enable

3.1.3.6 SYS_PLL_CTRL_REG

偏移地址 : 0x0020			默认值: 0x6000_0281 @24MHz OSC, 0x1D89_D241 @26MHz OSC, 0x6000_0181 @40MHz OSC, 0x6000_01E1 @32MHz OSC
位置	**访问**	**默认值**	**描述**
31	R/W	0x0	PLL_ENABLE Enable or disable the system PLL. 0: Disable the system PLL 1: Enable the system PLL

			Note: *The PLL frequency F_{output} = (F_{hosc}* N.f) / M, the output clock must be in range of 960MHz.* *The default value is set for 960MHz with 40MHz OSC.*
30:29	RW	0x3	DPLL_DITHER_DISABLE
28:13	RW	0x0000	DPLL_FRAC *Note : V_{FRAC} = f * 2^{16}*
12	RW	0x0	DPLL_FRAC_CTRL
11:4	RW	0x18	DPLL_NDIV
3:0	RW	1	FACTOR_M PLL factor M (1 ~ 8). M = Factor *Note: when the factor is set to 0, M will be set to 1*

3.1.3.7 SYS_CLK1_CTRL_REG

偏移地址 : 0x0024			**默认值: 0x0000_0201**
位置	**访问**	**默认值**	**描述**
31:25	/	/	/
24	R/W	0x0	ROM_READ_TWO_CYCLES_MODE 0: one cycle ROM read. 1: two cycles ROM read
23:18	/	/	/
17:16	R/W	0x0	CPU_CLK_SRC_SEL CPU clock source select 00: HFCLK(default) 01: LFCLK 1x: SYSCLK1
15:11	/	/	/
10:8	RW	0x2	FACTOR_M PLL factor M (4~7,9) 0~3: M= Factor + 4 4: M=9 5~7: reserved
7:4	/	/	/
3:0	RW	0x1	FACTOR_N PLL factor N (1 ~ 16). Factor = 0~15

			N = Factor + 1 ***Note:*** *$F_{sysclk1}$ = 960MHz/ M/N, the default value is 80MHz.*

3.1.3.8 SYS_CLK3_CTRL_REG

偏移地址 : 0x002C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	RW	0	SYS_CLK3_EN 1: enable the clock of system 3 0: disable the clock of system 3 ***Note:*** *F_{sysclk} = F_{src}/ N, the clock is fixed to 160MHz.*
30:1	/	/	/
0	RW	0	WLAN_WUP_BY_HOSC 1: WLAN wake up from SLEEP mode using HOSC 0: WLAN wake up from SLEEP mode using LOSC

3.1.3.9 DEV_CLK_CTRL_REG

偏移地址 : 0x0034			**默认值: 0x0003_0001**
位置	**访问**	**默认值**	**描述**
31	RW	0	CKADC_AUD_EN 1: enable the audio codec ADC clock 0: disable the audio codec ADC clock
30:24	/	/	/
23	RW	0	CKCLD_AUD_EN 1: enable the audio class-D clock 0: disable the audio class-D clock
22:21	/	/	/
20:16	RW	3	CKCLD_FACTOR_N PLL factor N (4 ~ 32). Factor = 3~31 N = Factor + 1 *Note: F_{ckcld} = 960MHz/2/N, the default value is 120MHz. this clock is used as a source clock for class-D.*
15:11	/	/	/
10:8	RW	0x0	DEV1_FACTOR_M PLL factor M (4~7,9) 0~3: M= Factor + 4

			4： M=9 5~7: reserved
7:4	/	/	/
3:0	RW	0x1	DEV1_FACTOR_N PLL factor N (1 ~ 16). Factor = 0~15 N = Factor + 1 *Note: $F_{devclk1}$ = 960MHz/ M/N, the default value is 96MHz. this clock is used as a source clock for some devices.*

3.1.3.10 DCXO_CTRL0_REG

偏移地址 : 0x0058			**默认值: 0x9409_0B00**
位置	**访问**	**默认值**	**描述**
31	RW	1	DCXO_EN DCXO Enable 0: disable 1: enable
30	/	/	/
29:28	RW	1	CLK_MODE_SEL Clock Mode Select (When AUTO_DET_EN is disable) 00: Internal Clock 01: Crystal 10: Analog 11: Digital
27:20	RW	0x40	FRE_TRI Frequency Trimming
19	RW	1	ALC_EN ALC Enable 0: disable 1: enable
18:17	/	/	/
16:12	RW	0x10	ICTRL BIAS Current Control
11	RW	1	RF_DIG_REF_CLK_EN 0: disable 1: enable

10	/	/	/
9	RW	1	BUFFER_DPLL_EN 0: disable 1: enable
8:6	/	/	/
5:4	R	xx	DCXO_DET 00: Internal clock 01: Crystal 10: Analog 11: Digital
3:1	/	/	/
0	RW	0	AUTO_DET_EN Auto Detect Enable 0: disable 1: enable

3.1.3.11 CONN_BOOT_FLAG_REG

偏移地址 : 0x0070			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	WR	0	CONN_BOOT_FLAG Connect mode flag 1: Connect mode 0: IOT mode

3.1.3.12 POWERCTRL_CFG_REG

偏移地址 : 0x0074			**默认值: 0x0000_05CE**
位置	**访问**	**默认值**	**描述**
31:14	/	/	/
13	RW	0	BT_RSTN_HIGHLVEL_WAKEUP 0: Wakeup when found posedge of BT_RSTN. 1: Wakeup when found high level of BT_RSTN.
12	RW	0	WLAN_IRQ_HIGHLVEL_WAKEUP 0: WLAN_IRQ could only wakeup powerctrl through WIC. 1: Wakeup when found high level of WLAN_IRQ while BT_RSTN was low.
11	RW	0	IGNORE_WICWAKEUP

			0: WIC WAKEUP could take into effect at any time. 1: WIC WAKEUP couldn't take into effect when BT_RSTN was low.
10	RW	1	IGNORE_WICENACK 0: Use WICENACK in sleep/wakeup process. 1: Don't use WICENACK in sleep/wakeup process.
9	RW	0	WAKEUP_MODE 0: Wakeup when found posedge of interrupt. 1: Wakeup when found high level of interrupt.
8	RW	1	RTC_ALARM_WUP_TO_POWERCTRL 0: RTC alarm0/1 interrupt could not wake up powerctrl directly.. 1: RTC alarm0/1 interrupt could wake up powerctrl directly.
7:6	RW	11	RCOSC_CALIB_START_SRC RCOSC Calibration Start Source. 00：APP sleep 01：WLAN sleep 10：APP and WLAN sleep 11：LDO1 shut down
5	RW	0	CPU_SLEEP_NO_RETENTION 0: When CPU goto sleep mode, APP RAM could be retention. 1: When CPU goto sleep mode, no need to retention APP RAM.
4	RW	0	BT_SLEEP_RETENTION_OVR 0: BT reset retention should not overwrite CPU retention. 1: BT reset retention could overwrite CPU retention.
3	RW	1	BLE_SLEEP_TIMER_IRQ_TO_POWERCTRL 0: BLE Sleep Timer interrupt could not wake up powerctrl directly.. 1: BLE Sleep Timer interrupt could wake up powerctrl directly.
2	RW	1	WUPTIMER_IRQ_TO_POWERCTRL 0: Wakeup Timer interrupt could not wake up powerctrl directly.. 1: Wakeup Timer interrupt could wake up powerctrl directly.
1	RW	1	WUPIO_IRQ_TO_POWERCTRL 0: Wakeup IO interrupt could not wake up powerctrl directly.. 1: Wakeup IO interrupt could wake up powerctrl directly.
0	RW	0	BT_RSTN_WAKEUPPIN 0: BT reset PAD could not be used as wake up pin. 1: BT reset PAD could be used as wake up pin, positive edge means wake up, negetive edge means goto sleep.

3.1.3.13 SYS1_CTRL_REG

偏移地址 ：0x0080			默认值: 0x0000_0003
位置	**访问**	**默认值**	**描述**
31:18	/	/	/
17	R		WLAN_RSTN_STATU The WRSTN PIN status in connect mode 0: WLAN reset signal hold 1: WLAN reset signal release
16	R	/	BLE_RSTN_STATU The BRSTN PIN status in connect mode 0: BLE reset signal hold 1: BLE reset signal release
15:2	/	/	/
1	R	/	AR800A_RSTN_STATU system 1 Reset 1: release the global reset signal of the system 1 0: hold the global reset signal of the system 1
0	R	/	SYS1_RST_RSTN_STATU system 1 Reset 1: release the global reset signal of the system 1 0: hold the global reset signal of the system 1

3.1.3.14 SYS1_STA_REG

偏移地址 ：0x0084			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R	0	CPU_SLEEP 1: the CPU of system 1 is in SLEEP mode 0: the CPU of system 1 is not in SLEEP mode
1	R	0	CPU_SLEEPDEEP 1: the CPU of system 1 is in SLEEPDEEP mode 0: the CPU of system 1 is not in SLEEPDEEP mode
0	R	0	SUBSYS1_ALIVE 1: system 1 is alive

			0: system 1 is down

3.1.3.15 SYS3_CTRL_REG

偏移地址 : 0x0090			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:17	/	/	/
16	RW	0	WLAN_RSTN_CONN Wlan SW reset in connect mode 1: release the SW reset of WLAN in connect mode 0: hold the SW reset of WLAN in connect mode
15:2	/	/	/
0	RW	0	SYS3_RST System 3 Reset 1: release the global reset of the system 3 0: hold the global reset of the system 3

	Read	Write
AR400A	R	W

3.1.3.16 SYS3_STA_REG

偏移地址 : 0x0094			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R	0	CPU_SLEEP 1: the CPU of system 3 is in SLEEP mode 0: the CPU of system 3 is not in SLEEP mode
1	R	0	CPU_SLEEPDEEP 1: the CPU of system 3 is in SLEEPDEEP mode 0: the CPU of system 3 is not in SLEEPDEEP mode
0	R	0	SYS3_ALIVE 1: system 3 is alive 0: system 3 is down

Table 3- 1 System 3 Status Register

3.1.3.17 SYS1_WAKEUP_CTRL_REG

偏移地址 ：0x0098			默认值: 0x0000_000F
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	RW	1	VDDIO_SIP_SW_EN 1: VDDIO_SIP SW is enabled 0: VDDIO_SIP SW is closed
0	RW	1	SYS1_WAKEUP_LDO1_ON 1: LDO1 will be enabled when waking up the system 1 0: keep the LDO with its current state

3.1.3.18 SYS1_SLEEP_CTRL_REG

偏移地址 ：0x00A0			默认值: 0x8000_0002
位置	**访问**	**默认值**	**描述**
31	RW	1	WLAN_SRAM_96K_SWM8 _MODE WLAN SRAM(96k bytes) retention power switch (SWM8) mode 0: always on 1: SRAM switch maybe off
30	RW	0	CACHE_BLE_SRAM_48K_SWM7 _MODE CACHE/BLE SRAM(48k bytes) retention power switch (SWM7) mode 0: always on 1: SRAM switch maybe off
29	RW	0	SRAM_16K_SWM6 _MODE SRAM(16k bytes) retention power switch (SWM6) mode 0: always on 1: SRAM switch maybe off
28	RW	0	SRAM_16K_SWM5 _MODE SRAM(16k bytes) retention power switch (SWM5) mode 0: always on 1: SRAM switch maybe off
27	RW	0	SRAM_32K_SWM4 _MODE

			SRAM(32k bytes) switch (SWM4) mode 0: always on 1: SRAM switch maybe off
26	RW	0	SRAM_64K_SWM3 _MODE SRAM(64k bytes) switch (SWM3) mode 0: always on 1: SRAM switch maybe off
25	RW	0	SRAM_96K_SWM2 _MODE SRAM(96k bytes) switch (SWM2) mode 0: always on 1: SRAM switch maybe off
24	RW	0	SRAM_32K_SWM1 _MODE SRAM(32k bytes) switch (SWM1) mode 0: always on 1: SRAM switch maybe off
23:8	/	/	/
7:2	/	/	/
1	RW	1	SYS1_SLEEP_SW1_OFF 1: SW1 will be disabled when the system 1 goes into the deep-sleep mode 0: keep the power switch with its current state
0	RW	0	SYS1_SLEEP_LDO1_OFF 1: LDO1 will be disabled when the system 1 goes into the deep-sleep mode 0: keep the power switch with its current state

3.1.3.19 DCXO_STABLE_REF_TIME_REG

偏移地址 ：0x00A8			**默认值: 0x8000_0080**
位置	**访问**	**默认值**	**描述**
31:10	/	/	/
9:0	RW	0x80	DCXO Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 500us* *Set Value = 14us * 128 = 1.8ms*

3.1.3.20 DPLL_STABLE_REF_TIME_REG

偏移地址 ：0x00AC			默认值: 0x0000_000C
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	RW	0xC	DPLL Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 50us* *Set Value = 14us * 12 =168us*

3.1.3.21 LDO_STABLE_REF_TIME_REG

偏移地址 ：0x00B0			默认值: 0x0000_030D
位置	**访问**	**默认值**	**描述**
31:12	/	/	/
11：8	RW	0x3	RfipLdoDig Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 10us* *Set Value = 14us * 3 = 42us*
7:0	RW	0xD	LDO Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 60us* *Set Value = 14us * 13 = 182us*

3.1.3.22 DIGITAL_SWITCH_REF_TIME_REG

偏移地址 ：0x00B4			默认值: 0x3000_0002
位置	**访问**	**默认值**	**描述**
31:16	RW	0x3000	Reset Up Reference Time *REF_TIME = T_{HFCLK} * n* *Typical Value >= 12288 cycles* *Set Value = 25ns * 12288 = 300us (@40MHz OSC)*
15:0	RW	0x2	Digital Switch Reference Time *REF_TIME = T_{HFCLK} * n* *Typical Value >= 2 cycles* *Set Value = 25ns * 2 = 50ns (@40MHz OSC)*

3.1.3.23 RTC_LDO_VOL_CTRL_REG

偏移地址 ：0x00B8			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:19	/	/	0
18:16	RW	0	RTC LDO work Voltage Control 0: 1.075V 1: 0.975V 2: 0.875V 3: 0.775V 4: 0.675V 5: 0.60V 6: 1.175V 7: 1.275V
15:3	/	/	/
2:0	RW	0	RTC LDO Retention Voltage Control 0: 1.075V 1: 0.975V 2: 0.875V 3: 0.775V 4: 0.675V 5: 0.60V 6: 1.175V 7: 1.275V

3.1.3.24 BG_STABLE_REF_TIME_REG

偏移地址 ：0x00BC			默认值: 0x0000_0017
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	RW	0x17	LDO Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 100us* *Set Value = 14us * 23 = 322us*

3.1.3.25 DCDC_STABLE_REF_TIME_REG

偏移地址 ：0x00C0			默认值: 0x0080_000C
位置	**访问**	**默认值**	**描述**
31:26	/	/	/

25:16	RW	0x80	LDO to PWM Mode Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 500us* *Set Value = 14us * 128 = 1.8ms*
15:10	/	/	/
9:0	RW	0xC	Other Work Mode Switch Stable Reference Time *REF_TIME = T_{LFCLK} * n* *Typical Value <= 50us* *Set Value = 14us * 16 = 168us*

3.1.3.26 BLE_RTC_RST_CTRL_REG

偏移地址 : 0x00D0			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	RW	0	BLE_RTC_RST_RST BLE RTC Reset 1: release the global reset of the BLE RTC 0: hold the global reset of the BLE RTC

3.1.3.27 BLE_RTC_RST_CTRL_REG

偏移地址 : 0x00D4			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	RW	0	BLE_32M_CLK_EN BLE 32M clock enable 0：disable 1: enable
0	RW	0	BLE_48M_CLK_EN BLE 48M clock enable 0：disable 1: enable

3.1.3.28 RFAS_CTRL_REG

偏移地址 : 0x00D8			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/

0	RW	0	RFAS_RST RFAS Reset 1: release the global reset of RFAS 0: hold the global reset of RFAS

3.1.3.29 AR800A_BOOT_FLAG_REG

偏移地址 : 0x0100			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	RW	0	BOOT_FLAG_WRITE_LOCK 0x429B: AR800A_BOOT_FLAG filed is writable other: AR800A_BOOT_FLAG filed is read only ***Note:*** *The field of AR800A_BOOT_FLAG only can be changed when this bit is set to* ***0x429B****. In one write operation, the GRPCM will check this field whether equals to 0x429B. If not, the value of AR400A_BOOT_FLAG will be ignored.* *This field is always read with value 0x0000.* *Examples:* 1. After write 0x429B0001, then read value = 0x00000001 2. After write 0x11110000, then read value = 0x00000001 After write 0x429B0000, then read value = 0x00000000
15:4	/	/	/
3:0	RW	0	AR800A_BOOT_FLAG 0: boot from cold reset(default) 1: boot from deep sleep 2: boot for system update 3: boot for recovery others: reserved

3.1.3.30 AR800A_BOOT_ADDR_REG

偏移地址 : 0x0104			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	AR800A_BOOT_ADDR

3.1.3.31 AR800A_BOOT_ARG_REG

偏移地址 ：0x0108			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_BOOT_ARG

3.1.3.32 AR800A_PRIV_REG0

偏移地址 ：0x010C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_PRIV_REG0

3.1.3.33 AR800A_PRIV_REG1

偏移地址 ：0x0110			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_PRIV_REG1

3.1.3.34 AR800A_PRIV_REG2

偏移地址 ：0x0114			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_PRIV_REG2

3.1.3.35 AR800A_PRIV_REG3

偏移地址 ：0x0118			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_PRIV_REG3

3.1.3.36 AR800A_PRIV_REG4

偏移地址 ：0x011C			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	RW	0	AR800A_PRIV_REG4

3.1.3.37 AR800A_WAKE_TIMER_CNT_REG

偏移地址 ：0x0120			默认值: 0x0000_0000
位置	访问	默认值	描述
31	RW	0	AR800A_WAKE_TIMER_EN

30:0	R	0	AR400A_WAKE_TIMER_CNT Note: This is a free running counter and when the value of this counter equals to the value of AR400A_WAKE_TIMER_VAL, a wakeup signal will be issued to the Wakeup Interrupt Controller. If AR400A_WAKE_TIMER_EN is set to '0', this counter will be reset to 0 and stop counting.

3.1.3.38 AR800A_WAKE_TIMER_VAL_REG

偏移地址 : 0x0124			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	RW	0	AR800A_WAKEUP_TIMER_IRQ_STATUS 0: the ar800a wakeup timer irq is not pending 1: the ar800a wakeup timer irq is pending Note: this is a write-1-to-clear register. This is an asynchronies operation and this bit will not become to '0' immediately after writing '1' to clear the irq state. We should read the register until the value of this bit becomes '0', which means the irq pending state is actually cleared.
30:0	RW	0	AR800A_WAKE_TIMER_VAL

3.1.3.39 AR800A_PRIV_REG5

偏移地址 : 0x0128			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	AR800A_PRIV_REG5

3.1.3.40 AR800A_PRIV_REG6

偏移地址 : 0x012C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0	AR800A_PRIV_REG6

3.1.3.41 AR800A_WAKE_IO_EN_REG

偏移地址 : 0x0130			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:30	/	/	/
29:16	/	0	AR800A_WAKEUP_IOx_MODE 1: Positive Edge 0: Negative Edge bit0- bit14: WUPIO0 – WUPIO13
15:14	/	/	/

13:0	RW	0	AR800A_WAKEUP_IOx_ENB 1: IOx wakeup detection enable 0: IOx wakeup detection disable bit0- bit14: WUPIO0 – WUPIO13

3.1.3.42 AR800A_WAKE_IO_DEB_CLK_REG

偏移地址 : 0x0134			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:28	RW	0x0	AR800A_WAKEUP_DEB_CLK_SET1 IO wakeup debounce clk1 select, the DEB_CLK1 frequency CLK_SEL1<=14, Freq=FCLK/(2^{CLK_SEL1}); CLK_SEL1==15, reserved.
27:24	RW	0x0	AR800A_WAKEUP_DEB_CLK_SET0 IO wakeup debounce clk0 select, the DEB_CLK0 frequency CLK_SEL0<=14, Freq=FCLK/(2^{CLK_SEL0}); CLK_SEL0==15, reserved.
23:16	/	/	/
15:14	/	/	/
13:0	RW	0x0	AR800A_WAKEUP_IOx_CLK _SEL 0: IOx select DEB_CLK0 1: IOx select DEB_CLK1 bit0- bit14: WUPIO0 – WUPIO13

3.1.3.43 AR800A_WAKE_IO_STA_REG

偏移地址 : 0x0138			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:14	/	/	/
13:0	RW	0	AR800A_WAKEUP_IOx_ST 1: wakeup event is detected on IOx 0: Nothing bit0- bit14: WUPIO0 – WUPIO13 *Note: Write 1 to clear the status*

3.1.3.44 AR800A_WAKE_IO_STA_REG

偏移地址 : 0x013C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:14	/	/	/

13:0	R/W1C	0	AR800A_WAKEUP_IOx_ST 1: IO Configure Hold Enable 0: IO Configure Hold Disable bit0- bit14: WUPIO0 – WUPIO13 Note: when enable the IO hold function, the configuration(IEN, OEN, PULL, ODAT) of the relative IO will be hold to the current state even if the GPIO controller is powered down or the origin configuration is modified.

3.1.3.45 AR800A_IO_WUP_GEN_REG

偏移地址 : 0x0140			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	RW	0	AR800A_IO_WUP_GEN 1: IO Wakeup interrupt Enable 0: IO Wakeup interrupt Disable

3.1.3.46 AR800A_WAKEUP_IO_DEB_CYCLES_REG

偏移地址 : 0x0144			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0x000000	AR800A_WAKEUP_IO_DEB_CYCLES0 Bit[4N+3:4*N] : IO[N] debounce cycles (N: 0~7) WUPIO0 – WUPIO7 First must select clock for debounce (configurate by register AR800A_WAKE_IO_DEB_CLK), finally the IO input debounce clock cycles is (DEBC_CYCLE[3:0]+1)+16.

3.1.3.47 AR800A_WAKEUP_IO_DEB_CYCLES1_REG

偏移地址 : 0x0148			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23:0	RW	0x000000	AR800A_WAKEUP_IO_DEB_CYCLES1 Bit[4(N-8)+3 : 4*(N-8)] : IO[N] debounce cycles (N:8~13) WUPIO8 – WUPIO13 First must select clock for debounce (configurate by register AR800A_WAKE_IO_DEB_CLK), finally the IO input debounce clock cycles is (DEBC_CYCLE[3:0]+1)+16.

3.1.3.48 LDO_MODE_SW_SEL_REG

偏移地址 ：0x0150			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	RW	0	SMPS_PFM_MODE 1: SMPS select PFM mode 0: SMPS select PWM mode
1	RW	0	DIG_LDO_LQ_MODE 1: SYS_LDO select lq mode 0: SYS_LDO select active mode
0	RW	1	SMPS_MODE_SW_SEL_ENABLE 1: SMPS PWM/PFM mode select by this register 0: SMPS PWM/PFM mode select by power control

3.1.3.49 SMPS_PARAM_CTRL_REG

偏移地址 ：0x0200			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:29	RW	0	SMPS_OCP DCDC over current protection threshold tuning default: 400mA
28:24	RW	0	SMPS_BGTR [4:1]: for DCDC BANDGAP trimming [0]: for OCP disable
23	/	/	/
22:16	RW	0	SMPS_FTR [4:0]: for switching frequency tuning [6:5]: for option to decrease frequency
15:8	RW	0	SMPS_TEST_ITEM_SEL
7:4	RW	0	SMPS_TEST_MODE
3:2	RW	0	SMPS_BYPASS 00, DCDC bypass disable 01, DCDC power pmos 1/6 bypass when PFM mode 1x, DCDC all power pmos bypass
1	/	/	/
0	R	0	SMPS_WORK_MODE 0: PWM Mode

			1: PFM Mode *Note: the DCDC starts up from PWM mode by default.* *This field is read-only and can only be changed by **POWERCTRL** Module.*

3.1.3.50 ANA_BG_REG

偏移地址 : 0x0204			**默认值: 0x0010_000X**
位置	**访问**	**默认值**	**描述**
31:21	RW	0	/
20:16	RW	0x10	BG Output Voltage Trimming
15:1	/	/	/
0	R	x	ANA_BG_PND_1V8 BG Power Up Enable *Note: this field can be only set by **POWERCTRL** module.*

3.1.3.51 DLDO_PARAM_REG

偏移地址 : 0x020C			**默认值: 0x0808_0000**
位置	**访问**	**默认值**	**描述**
31:20	/	/	/
19	RW	1	TESTPEAK_LDO1 enable the auxiliary circuit to avoid output large ripple during select LDO work 1: enable 0: disable Note: this field is set by POWERCTRL module
18	R	0	STARTICC_LDO1 decrease over current protection threshold at start up 1: enable 0: disable Note: this field is set by POWERCTRL module
17	RW	0	TESTICC_LDO over current protection enable 1: enable 0: disable Note: this field is set by POWERCTRL module
16	R	0	LDO1_LQ_MODE_EN

			LDO1 LQ mode enable 1: enable 0: disable Note: this field is set by POWERCTRL module
15:12	/	/	/
11:8	RW	0	BG_OUTPUT_TRIM BG output trimming Note: eFuse override
7:1	/	/	/
0	R	0	BG_PWR 0: disable 1: enable Note: This field is set by POWERCTRL module and must be enable before enabling DIG_LDO.

3.1.3.52 CFG_IO_ST_REG

偏移地址 ：0x0214			**默认值: 0x0000_000X**
位置	**访问**	**默认值**	**描述**
31:2	RW	0	/
1	R	x	SIP IO 0: no flash sip 1: with flash sip in package / | Read | Write AR400A | R | -
0	/	/	/

3.1.3.53 CPU_RST _SRC_REG

偏移地址 ：0x0218			**默认值: 0x0000_000X**
位置	**访问**	**默认值**	**描述**
31:11	/	/	/
10:9	RW	0	IS_WATCHDOG_CPU_RST The CPU reset source is watchdog(only reset CPU) output. Write 2’b11 clear these bits. 00: no 01: one time watchdog(only reset CPU) 10: two times watchdog(only reset CPU) 11: three times watchdog(only reset CPU)
8	RW	0	IS_WATCHDOG_ALL_RST

			The CPU reset source is watchdog(reset all system) output. Write 1 clear this bit. 0: no 1: yes
7:2	/	/	/
1	RW	0	IS_PMU_RST The CPU reset source is digital PMU output. Write 1 clear this bit. 0: no 1: yes
0	RW	0	IS_PWRON_RST The CPU reset source is POWER ON or P_RESETn. Write 1 clear this bit. 0: no 1: yes

3.1.3.54 WLAN_HIF_OV_CTRL_REG

偏移地址 : 0x021C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	WLAN_IRQ_OVER_HIF: use wlan_irq generated in WLAN_MISC logic to replace the corresponding output of WLAN_HIF 0: not override WLAN_HIF output 1: override WLAN_HIF output
6	R/W	0	WLAN_WUP_OVR_HIF: use WLAN_WUP(bit2) to override the corresponding output of WLAN_HIF 0: not override WLAN_HIF output 1: override WLAN_HIF output
5	R/W	0	RESET_CPU_OVR_HIF: use RESET_CPU(bit1) to override the corresponding output of WLAN_HIF 0: not override WLAN_HIF output 1: override WLAN_HIF output
4	R/W	0	DISABLE_CPU_CLK_OVR_HIF: use DISABLE_CPU_CLK(bit0) to override the corresponding output of WLAN_HIF 0: not override WLAN_HIF output 1: override WLAN_HIF output
3	/	/	Reserved
2	R/W	0	WLAN_WUP: wake-up wlan from sleep mode, host firmware need to clear it after WLAN waked up
1	R/W	1	RESET_CPU: reset WLAN CPU 0: release WLAN CPU reset 1: WLAN CPU is reset

0	R/W	1	DISABLE_CPU_CLK: disable WLAN CPU clock 0: wlan cpu clock enable 1: wlan cpu clock disable

3.1.3.55 SRAM_BIST_CFG_REG

偏移地址 ：0x0220			默认值: 0x2222_2222
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23:16	RW	0x22	ARM_SINGLE_PORT_SRAM_CFG ram_cfg[7:0] bit [2:0]: connect to EMA bit [4:3]: connect to EMAW others : reserved
15:8	RW	0x22	ARM_DAUL_PORT_SRAM_CFG ram_cfg[7:0] bit [2:0]: connect to EMAA bit [6:4]: connect to EMAB others : reserved
7:0	RW	0x22	SYNOPSYS_SRAM_CFG ram_cfg[7:0] bit [0]: connect to REME bit [3]: connect to TEST1 bit [7:4]: connect to REM others : reserved

3.1.3.56 WLAN_SRAM_SHARE_REG

偏移地址 ：0x0224			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6:0	RW	0x0	WLAN_SRAM_SHARE 0000000: No share APP SRAM 0000001: share 16K bytes APP SRAM 0000011: share 32K bytes APP SRAM 0000111: share 64K bytes APP SRAM 0001111: share 96K bytes APP SRAM 0011111: share 128K bytes APP SRAM 0100000: share APP SRAM with connect mode, total 128k bytes. WLAN DTCM: 48k bytes (0x04000000~0x0400BFFF) WLAN AHB: 80k bytes (0x0800C000~0x0801FFFF)

			WLAN PAS: 48k bytes (0x0900C000~0x09017FFF) 1000000: BLE share 128k bytes for debug mode Others: reserved

3.1.3.57 BLE_SRAM_SHARE_CTRL_REG

偏移地址 : 0x0228			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	RW	0x0	BLE_SRAM_SHARE_CTRL 0: APP(Cache) use shared 16K SRAM 1: BLE use shared 16K bytes SRAM

3.1.3.58 LPUART0_WAKEUP_CTRL_REG

偏移地址 : 0x0230			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	RW	0	LPUART0_WAKEUP_ENABLE 0: the module clock is gated off 1: the module clock is released to work
30:18	/	/	/
17:16	RW	0x0	LPUART0_WAKEUP_IN_SEL 0: LPUART0 wakeup input use UART0 serial in 1: LPUART0 wakeup input use UART1 serial in 2: LPUART0 wakeup input use UART2 serial in 3: reserved
15:1	/	/	/
0	RW	0x0	LPUART0_CLK_SEL 0: LPUART0 wakeup clock use LFCLK 1: LPUART0 wakeup clock use HFCLK (used for test)

3.1.3.59 LPUART1_WAKEUP_CTRL_REG

偏移地址 : 0x0234			**默认值: 0x0001_0000**
位置	**访问**	**默认值**	**描述**
31	RW	0	LPUART1_WAKEUP_ENABLE 0: the module clock is gated off 1: the module clock is released to work
30:18	/	/	/
17:16	RW	0x1	LPUART1_WAKEUP_IN_SEL

			0: LPUART1 wakeup input use UART0 serial in 1: LPUART1 wakeup input use UART1 serial in 2: LPUART1 wakeup input use UART2 serial in 3: reserved
15:1	/	/	/
0	RW	0x0	LPUART1_CLK_SEL 0: LPUART1 wakeup clock use LFCLK 1: LPUART1 wakeup clock use HFCLK (used for test)

3.1.3.60 GPADC_CLK_CTRL_REG

偏移地址 ：0x0238			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: LFCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.1.3.61 32K_CLK_CTRL_REG

偏移地址 ：0x023C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:4	/	/	/
3	R/W	0	WLAN_32K_SEL 0: select rco_losc_mux_clk as wlan function clock 1: select rco_calib_clk as wlan function clock
2	R/W	0	WUP_TIMER_32K_SEL 0: select rco_losc_mux_clk as wake-up timer function clock 1: select rco_calib_clk as wake-up timer function clock

3.1.3.62 WKUP_SRC_BUS_CLK_CTRL_REG

偏移地址 ：0x0240			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	RW	0x0	RCCAL_CLK_GATING 0: the clock is gated off 1: the clock is running
6	RW	0x0	GPADC_CLK_GATING 0: the clock is gated off 1: the clock is running
5	/	/	/
4			LPUART1_WKUP_CLK_GATING 0: the clock is gated off 1: the clock is running
3	/	/	/
2	R/W	0x0	LPUART0_WKUP_CLK_GATING 0: the clock is gated off 1: the clock is running
1:0	/	/	/

3.1.3.63 WKUP_SRC_RST_CTRL_REG

偏移地址 ：0x0244			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/

7	RW	0x0	RCCAL_RSTN 0: the module is in reset state 1: the module is released to work
6	RW	0x0	GPADC_RSTN 0: the module is in reset state 1: the module is released to work
5	/	/	/
4	RW	0x0	LPUART1_WAKEUP_RSTN 0: the module is in reset state 1: the module is released to work
3	/	/	/
2	RW	0x0	LPUART0_WAKEUP_RSTN 0: the module is in reset state 1: the module is released to work
1:0	/	/	/

3.1.3.64 FLASH_ENCRYPT_AES_NONCE0_REG

偏移地址 : 0x0250			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	RW	0x0	FLASH_ENCRYPT_AES_NONCE0 Flash encrypt module AES nonce bit[31:0]. These bits only changed one time after system power up.

3.1.3.65 FLASH_ENCRYPT_AES_NONCE1

偏移地址 : 0x0254			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
15:0	RW	0x0	FLASH_ENCRYPT_AES_NONCE1 Flash encrypt module AES nonce bit[47:32]. These bits only changed one time after system power up.

3.1.3.66 BLE_RCOSC_CALIB_REGr0_REG

偏移地址 : 0x0260			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:30	/	/	/
29	RW	0x0	RCO_CALIB_EN RCOSC calibration function enable 1: enable

			0: disable
28	RW	0x0	RCO_CALIB_RST_PUL When write 1 to this bit, reset RCOSC calibration then run again, when write 0, no effect. It is always read as 0.
27	/	/	/
26:24	R	0x0	RCO_CALIB_CS RCOSC calibration current state. It is read only. 000: IDLE 001: WAIT_DCXO_READY 011: WAIT_CAL_FINISH 110: CAL_FINISH 010: WAIT_TIMER Others: reserved
23:21	/	/	/
20	RW	0x0	RCO_CALIB_SW_REQ_PUL When write 1 to this bit, begin RCOSC calibration process at once, when write 0, no effect. It is always read as 0.
19:17	/	/	/
16	RW	0x0	RCO_WUP_TIME_EN RCOSC calibration periodically wake-up function enable 1: enable 0: disable
15:13	/	/	/
12:0	RW	0x0	RCO_WUP_TIME RCO_SLP calibration periodically wake-up time. Configure by software to wake up system, and begin RCO_SLP calibration process. The time unit of RCO_WUP_TIME is 32Khz(divided from RCO_SLP).

3.1.3.67 BLE_RCOSC_CALIB_REG1

偏移地址 : 0x0264			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:20	/	/	/
19:16	RW	0x0	RCO_SCALE_PHASE2_NUM wake-up times in phase2
15:12	RW	0x0	RCO_SCALE_PHASE1_NUM wake-up times in phase1

11	/	/	/
10:8	RW	0x0	RCO_SCALE_PHASE3_WUP_TIMES multiply factor of RCO_WUP_TIME in wake-up phase3 0x0: 10 times 0x1: 16 times 0x2: 20 times 0x3: 24 times 0x4: 32 times 0x5: 40 times 0x6: 64 times 0x7: 128 times
7	/	/	/
6:4	RW	0x0	RCO_SCALE_PHASE2_WUP_TIMES multiply factor of RCO_WUP_TIME in wake-up phase2 0x0: 2 times 0x1: 4 times 0x2: 6 times 0x3: 8 times 0x4: 10 times 0x5: 12 times 0x6: 14 times 0x7: 16 times
3:2	/	/	/
1	RW	0x0	RCO_NORMAL_WUP_TIMES_SEL In normal wake up mode, actual wake-up time is the multiply of RCO_WUP_TIME * factor 1: select RCO_SCALE_PHASE3_WUP_TIMES as the multiply factor of RCO_WUP_TIME 0: select RCO_SCALE_PHASE2_WUP_TIMES as the multiply factor of RCO_WUP_TIME
0	RW	0x0	RCO_WUP_MODE_SEL Scale wake up and Normal wake up are two wake up methods 1: select scale wake up method 0: select normal wake up method

3.1.3.68 BLE_CLK32K_SWITCH_REG0

偏移地址 : 0x0268			**默认值: 0x0271_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	/
25:16	RW	0x271	DIV_HALFCYCLE_TARGET

			Bit[9:0], The target half cycle number for 32kHz clock divide
15:5	/	/	/
4	RW	0x0	DIV_CLK_EN The 32KHz divider enable 1: enable 0: disable
3	RW	0x0	SYS_32K_SEL The source of 32kHz clock select 1: the clock from RCOSC Calibration output 0: the RCOSC/LFCLK output
2	RW	0x0	BLE_SEL_RCCAL_32K The source of 32kHz clock select 1: the clock from RCOSC Calibration output 0: the RCOSC/LFCLK output
1	RW	0x0	DIV_CLK_SRC_SEL The source clock select for divide to 32KHz clock 1: 32MHz Clock 0: HFCLK
0	RW	0x0	CLK32K_AUTO_SW_EN 32K clock auto switch enable. 1: enable 0: disable

3.1.3.69 BLE_CLK32K_SWITCH_REG1

偏移地址 : 0x026C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:27	/	/	/
26:16	R	0x0	CLK32K_SW_OFFSET_DOWN The offset when switch from divide 32k clock to 32KHz input clock
15:11	/	/	/
10:0	R	0x0	CLK32K_SW_OFFSET_ON The offset when switch from 32KHz input clock to divide 32k clock

3.2 时钟控制单元（CCM）

3.2.1 概述

CCMU 模块管理各模块的复位和时钟，并提供各模块的配置以调整各模块的时钟。

3.2.2 CCM 寄存器列表

模块名	基地址	
Clock Control Module	0x40040400	
寄存器名	**偏移地址**	**描述**
CPU_BUS_CLKCFG_REG	0x0000	CPU BUS Clock Configure Register
BUS_CLK_GATING_CTRL_REG	0x0004	Bus Clock Gating Control Register
BUS_DEV_RST_CTRL_REG	0x0008	Bus Device Reset Control Register
SPI0_CLK_CTRL_REG	0x0020	SPI0 Clock Control Register
SS_CLK_CTRL_REG	0x002C	SS Clock Control Register
AUDIO_CLK_CTRL_REG	0x0034	Audio Clock Control Register
IRRX_CLK_CTRL_REG	0x0038	IRRX Clock Control Register
IRTX_CLK_CTRL_REG	0x003c	IRTX Clock Control Register
SYSTICK_REFCLK_CTRL_REG	0x0040	System Tick Reference Clock Register
SYSTICK_CALIB_CTRL_REG	0x0044	System Tick Clock Calibration Register
PCLK_SPC_MCLK_CTRL_REG	0x005C	Special APB Clock Control Register (UART/GPRCM/RTC APB bus clock)
PSRAM_CLK_CTRL_REG	0x0060	PSRAM clock control register
KEYSCAN_CLK_CTRL_REG	0x0064	Keyscan clock control register

3.2.3 CCM 寄存器描述

3.2.3.1 CPU_BUS_CLKCFG_REG

偏移地址 : 0x0000			**默认值: 0x0000_0001**
位置	**访问**	**默认值**	**描述**
31:10	/	/	/
9:8	R/W	0x0	AHB2_CLK_DIV 00: /1 01: /2 10: /3 11: /4
7:6	/	/	/
5:4	R/W	0x0	APB_CLK_SRC_SEL

			APB bus clock source select 00: HFCLK 01: LFCLK 1X: AHB2 Clock
3:2	/	/	/
1:0	R/W	1	APB_CLK_DIV 00: /1 01: /2 10: /4 11: /8

3.2.3.2 BUS_CLK_GATING_CTRL_REG

偏移地址 ：0x0004			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W S+	0	SMCARD_CLK_GATING 0: the clock is gated off 1: the clock is running
30	R/W S+	0	TRNG_CLK_GATING 0: the clock is gated off 1: the clock is running
29	R/W S+	0	AUDIO_CODEC_CLK_GATING 0: the clock is gated off 1: the clock is running
28	R/W S+	0	UART2_CLK_GATING 0: the clock is gated off 1: the clock is running
27	R/W S+	0	GPIO_CLK_GATING 0: the clock is gated off 1: the clock is running
26	R/W	0	KEYSCAN_CLK_GATING 0: the clock is gated off 1: the clock is running

25	/	/	/
24	R/W	0	IRRX_CLK_GATING 0: the clock is gated off 1: the clock is running
23	R/W	0	IRTX_CLK_GATING 0: the clock is gated off 1: the clock is running
22	R/W S+	0	DAUDIO_CLK_GATING 0: the clock is gated off 1: the clock is running
21	R/W	0	PWM_ECT_CLK_GATING 0: the clock is gated off 1: the clock is running
20	/	/	/
19	R/W S+	0	TWI1_CLK_GATING 0: the clock is gated off 1: the clock is running
18	R/W S+	0	TWI0_CLK_GATING 0: the clock is gated off 1: the clock is running
17	R/W S+	0	UART1_CLK_GATING 0: the clock is gated off 1: the clock is running
16	R/W S+	0	UART0_CLK_GATING 0: the clock is gated off 1: the clock is running
15	R/W	0	BLE_CLK_GATING 0: the clock is gated off 1: the clock is running
14	R/W	0	DMA_SEC_CLK_GATING

	S+		0: the clock is gated off 1: the clock is running
13:9	/	/	/
8	R/W S+	0	FLASH_ENCRYPT_CLK_GATING 0: the clock is gated off 1: the clock is running
7	R/W S+	0	TZASC_CLK_GATING 0: the clock is gated off 1: the clock is running
6	R/W	0	DMA_CLK_GATING 0: the clock is gated off 1: the clock is running
5:4	/	/	/
3	R/W	0	FLASH _CTRL_CLK_GATING 0: the clock is gated off 1: the clock is running
2	R/W	0	SS_CLK_GATING 0: the clock is gated off 1: the clock is running
1	/	/	/
0	R/W S+	0	SPI0_CLK_GATING 0: the clock is gated off 1: the clock is running

说明

1. The type S+ means this bit can't change by non-secure access when corresponding module has set security in TZASC register.

3.2.3.3 BUS_DEV_RST_CTRL_REG

偏移地址 : 0x0008			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W S+	0	SMCARD_RST 0: the module is in reset state

			1: the module is released to work
30	R/W S+	1	TRNG_RST 0: the module is in reset state 1: the module is released to work. The default value is 1, used for TRNG retention registers.
29	R/W S+	0	AUDIO_CODEC_RST 0: the module is in reset state 1: the module is released to work
28	R/W S+	0	UART2_ RST 0: the module is in reset state 1: the module is released to work
27	/	/	/
26	R/W	0	KEYSCAN_RST 0: the module is in reset state 1: the module is released to work
25	/	/	/
24	R/W	0	IRRX_RST 0: the module is in reset state 1: the module is released to work
23	R/W	0	IRTX_RST 0: the module is in reset state 1: the module is released to work
22	R/W S+	0	DAUDIO_RST 0: the module is in reset state 1: the module is released to work
21	R/W	0	PWM_ECT_RST 0: the module is in reset state 1: the module is released to work
20	/	/	/
19	R/W S+	0	TWI1_ RST

			0: the module is in reset state 1: the module is released to work
18	R/W S+	0	TWI0_ RST 0: the module is in reset state 1: the module is released to work
17	R/W S+	0	UART1_ RST 0: the module is in reset state 1: the module is released to work
16	R/W S+	0	UART0_RST 0: the module is in reset state 1: the module is released to work
15	R/W	0	BLE_RST 0: the module is in reset state 1: the module is released to work
14	R/W S+	0	DMA_SEC_RST 0: the module is in reset state 1: the module is released to work
13	R/W	1	DCACHE_RST 0: the module is in reset state 1: the module is released to work
12:11	/	/	/
10	R/W	0	WLANC_RST 0: the module is in reset state 1: the module is released to work
9	/	/	/
8	R/W S+	0	FLASH_ENC_RST 0: the module is in reset state 1: the module is released to work
7	/	/	/
6	R/W	0	DMA_ RST

			0: the module is in reset state 1: the module is released to work
5:4	/	/	/
3	R/W	0	FLASH _CTRL_RST 0: the module is in reset state 1: the module is released to work
2	R/W	0	SS_ RST 0: the module is in reset state 1: the module is released to work
1	/	/	/
0	R/W S+	0	SPI0_ RST 0: the module is in reset state 1: the module is released to work
说明 1. The type S+ means this bit can't change by non-secure access when corresponding module has set security in TZASC register.			

3.2.3.4 SPI0_CLK_CTRL_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: DEVCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N

			clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.5 SS_CLK_CTRL_REG

偏移地址 ：0x002C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: DEVCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N Clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.6 AUDIO_CLK_CTRL_REG

偏移地址 ：0x0034			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23	R/W	0	DAUDIO_CLK_EN Daudio clock enable 0: disable 1: enable
22:17	/	/	/
16	R/W	0	DAUDIO_CLK_SEL Daudio clock source select 0: select ADC_CLK from DPLL 1: select CLASSD_CLK from DPLL
15:8	/	/	/
7	R/W	0	CODEC_CLK_EN Audio codec clock (ADC&ClassD clock) enable 0: disable 1: enable
6:3	/	/	/
2	R/W	0	CLASSD_CLK_SEL Codec class-D clock source selection 0: select CLASSD_CLK from DPLL 1: select outer I2S clock
1	R/W	0	ADC_CLK_SEL Codec ADC clock source selection 0: select ADC_CLK from DPLL 1: select outer I2S clock
0	R/W	0	OUTER_CLK_SEL Outer I2S clock source selection 0: I2S MCLK input 1: I2S BCLK input

3.2.3.7 IRRX_CLK_CTRL_REG

偏移地址 ：0x0038			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE

			0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: LFCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.8 IRTX_CLK_CTRL_REG

偏移地址 : 0x003C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: LFCLK 1x: reserved

23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.9 SYSTICK_REFCLK_CTRL_REG

偏移地址 : 0x0040			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: LFCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/

3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.10 SYSTICK_CALIB_CTRL_REG

偏移地址 ：0x0044			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	/
25	R/W	0	ST_NOREF 1: there is no reference clock 0: use the reference clock
24	R/W	0	ST_SKEW Note: set this bit to 0 if the system timer clock, the external reference clock, or FCLK as indicated by ST_NOREF, can guarantee an exact multiple of 10ms. Otherwise, set this bit to 1.
23:0	R/W	0	ST_10MS_COUNTER Note: This field provides an integer value to compute a 10ms (100Hz) delay from either the reference clock, or FCLK if the reference clock is not implemented. For example: No reference clock, FCLK=50MHz, CNT = 0x7A11F(49999) REFCLK = 1MHz, CNT = 0x270F(9999)

3.2.3.11 FLASH _SPI_CLK_CTRL_REG

偏移地址 ：0x0054			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: DEVCLK

			1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.12 PCLK_SPC_CLK_CTRL_REG

偏移地址 ：0x005C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: DEVCLK 10: FLCLK 11: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.13 PSRAM_OPI_CLK_CTRL_REG

偏移地址 ：0x0060			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/
25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: DEV1_CLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.2.3.14 KEYSCAN_CLK_CTRL_REG

偏移地址 ：0x0064			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	R/W	0	MCLK_ENABLE 0: the module clock is gated off 1: the module clock is released to work CLKm = CLKsrc / N / M
30:26	/	/	/

25:24	R/W	0	MCLK_SRC_SEL Clock source selection 00: HFCLK 01: LFCLK 1x: reserved
23:18	/	/	/
17:16	R/W	0	CLK_DIV_RATIO_N clock pre-divide ratio N. 00: N = 1 01: N = 2 10: N = 4 11: N = 8
15:4	/	/	/
3:0	R/W	0	CLK_DIV_RATIO_M Clock divide ratio M. M = value + 1 (1~16)

3.3 实时时钟(RTC)

3.3.1 概述

实时时钟(RTC)用于日历，是围绕一个48位计数器构建的，用于以“年-月-日”（YY-MM-DD）和“时-分-秒”（HH-MM-SS）的形式计算运行时间。当系统断电时，可通过备用电池进行操作。它有一个内置的闰年发生器。

在下电模式或正常运行模式下，闹钟（Alarm）在指定时间产生告警信号。在正常运行模式下，告警中断和电源管理唤醒都被激活。在下电模式下，电源管理唤醒信号被激活。在本节中，有两种闹钟。闹钟0 (Alarm 0）是通用警报器，它的计数器是基于秒的。闹钟1（Alarm 1）是以周为单位的实时闹钟。

3.3.2 RTC 寄存器列表

模块名	**基地址**	
Real Time Clock	0x40041800	
寄存器名	**偏移地址**	**描述**
RTC_CTRL_REG	0x0000	RTC Control Register
RTC_YYMMDD_REG	0x0010	RTC Year Month Day Register
RTC_HHMMSS_REG	0x0014	RTC Hour Minute Second Register

ALM0_CNT_REG	0x0020	Alarm 0 Counter Register
ALM0_CURVAL_REG	0x0024	Alarm 0 Current Value Register
ALM0_EN_REG	0x0028	Alarm 0 Enable Register
ALM0_IRQEN_REG	0x002C	Alarm 0 IRQ Enable Register
ALM0_IRQST_REG	0x0030	Alarm 0 IRQ Status Register
ALM1_WK_HHMMSS_REG	0x0040	Alarm 1 Week Hour-Minute-Second Register
ALM1_EN_REG	0x0044	Alarm 1 Enable Register
ALM1_IRQEN_REG	0x0048	Alarm 1 IRQ Enable Register
ALM1_IRQST_REG	0x004C	Alarm 1 IRQ Status Register
ALM_WAKEUP_EN_REG	0x0050	Alarm wakeup Enable Register
FRUN_CNT_L_REG	0x0060	Free Running Counter bit[31:0]
FRUN_CNT_H_REG	0x0064	Free Running Counter bit[47:32]

3.3.3 RTC 寄存器描述

3.3.3.1 RTC_ CTRL_REG

偏移地址 : 0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0x0	RTC_TEST_MODE_CTRL. RTC TEST Mode Control bit.
30	R/W	0x0	RTC_DEBUG. RTC Simulation Control bit 0: No effect. 1: simulation mode
29:2	/	/	/
1	R	0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After the RTC RTC_HHMMSS_ACCE is cleared, the writing operation of HH-MM-SS register should at most delay one sysrtc_32k cycle..
0	R	0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the RTC YY-MM-DD register, this bit is set and it will be cleared until the real writing operation is finished. After the RTC RTC_YYMMDD_ACCE is cleared, the writing operation

			of YY-MM-DD register should at most delay one sysrtc_32k cycle.

3.3.3.2 RTC_YYMMDD_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:25	/	/	/.
24	R/W	0x0	LEAP. Leap Year. 0: not 1: Leap year. This bit cannot be set by hardware. It should be set or cleared by software.
23:16	R/W	x	YEAR. Year. Range from 0~256.
15:12	/	/	/
11:8	R/W	x	MONTH. Month. Range from 1~12.
7:5	/	/	/.
4:0	R/W	x	DAY. Day. Range from 1~31. Note: If the written value is not from 1 to 31, it turns into 31 automatically. The month field and the year field are similar.

3.3.3.3 RTC_HHMMSS_REG

偏移地址 ：0x0014			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:29	R/W	0x0	WEEK_NO. Week number. 000: Monday 001: Tuesday

			010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/
20:16	R/W	x	HOUR. Range from 0~23
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59

3.3.3.4 ALM0_CNT_REG

偏移地址 : 0x0020			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	ALM0_CNT Alarm 0 Counter is based on second.

3.3.3.5 ALM0_CURVAL_REG

偏移地址 : 0x0024			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R	x	ALM0_CURVAL

3.3.3.6 ALM0_EN_REG

偏移地址 : 0x0028			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W	0	ALM0_EN If this bit is set to 1, the alarm 0 counter register’s valid bits will down

			count to 0 and the alarm pending bit will be set to 1 0: disable 1: enable

3.3.3.7 ALM0_IRQEN_REG

偏移地址 ：0x002C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W	0	ALM0_IRQEN 0: disable 1: enable

3.3.3.8 ALM0_IRQST_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W	0	ALM0_IRQST 0: no effect 1: pending

3.3.3.9 Alarm 1_WK_HHMMSS_REG

偏移地址 ：0x0040			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:21	/	/	/
20:16	R/W	X	HOUR Range from 0-23
15:14	/	/	/
13:8	R/W	X	MINUTE Range from 0-59
7:6	/	/	/
5:0	R/W	X	SECOND Range from 0-59

3.3.3.10 ALM1_EN_REG

偏移地址 ：0x0044			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6	R/W	0	SUN_ALM1_EN Sunday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 6, the alarm IRQ pending bit will be set to “1”.
5	R/W	0	SAT_ALM1_EN Saturday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 5, the alarm IRQ pending bit will be set to “1”.
4	R/W	0	FRI_ALM1_EN Friday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 4, the alarm IRQ pending bit will be set to “1”.
3	R/W	0	THU_ALM1_EN Thursday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 3, the alarm IRQ pending bit will be set to “1”.
2	R/W	0	WED_ALM1_EN

			Wednesday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 2, the alarm IRQ pending bit will be set to “1”.
1	R/W	0	TUE_ALM1_EN Tuesday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 1, the alarm IRQ pending bit will be set to “1”.
0	R/W	0	MON_ALM1_EN Monday Alarm 1 Enable 0: disable 1: enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 0, the alarm IRQ pending bit will be set to “1”.

3.3.3.11 ALM1_IRQEN_REG

偏移地址 : 0x0048			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W	0	ALM1_IRQEN 0: disable 1: enable

3.3.3.12 ALM1_IRQST_REG

偏移地址 : 0x004C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:1	/	/	/

0	R/W	0	ALM1_WEEK_IRQST Alarm 1 week(0-7) IRQ Pending 0: No effect 1: pending

3.3.3.13 ALM_WAKEUP_EN_REG

偏移地址 : 0x0050			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	R/W	0	ALM1_WAKEUP 0: disable alarm1 wakeup output 1: enable alarm1 wakeup output
0	R/W	0	ALM0_WAKEUP 0: disable alarm0 wakeup output 1: enable alarm0 wakeup output

3.3.3.14 FREERUN_CNT_L_REG

偏移地址 : 0x0060			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	Free Running Counter bit[31:0] Note: Free running counter is a 48-bit counter which is driven by LFCLK and starts to count as soon as the system reset is released and the LFCLK is ready. Write will reset the counter value.

3.3.3.15 FREERUN_CNT_H_REG

偏移地址 : 0x0064			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	Free Running Counter bit[47:32] Note: Free running counter is a 48-bit counter which is driven by LFCLK and starts to count as soon as the system reset is released and the LFCLK is ready. Write will reset the counter value.

3.4 通用定时器(Timer0/1)

3.4.1 概述

定时器0和1的输入源可以来自内部RC振荡器、外部32768Hz晶体或OSC。它旨在提供最大的准确性和有效的管理，即使系统处于长或短的响应时间。他们提供32位可编程溢出计数器，工作在自动重载模式或无重载模式。

3.4.2 Timer 寄存器列表

模块名	基地址	
Timer	0x40040800	
寄存器名	**偏移地址**	**描述**
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register

3.4.3 Timer 寄存器描述

3.4.3.1 TMR_IRQ_EN_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect 1: Timer 0 Interval Value reached interrupt enable.

3.4.3.2 TMR_IRQ_STA_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
1	R/W	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 0 interval value is reached.

3.4.3.3 TMR0_CTRL_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC.

			Timer 0 Clock Source. 00: LOSC, 01: HOSC. 10: / 11: /
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect, 1: Reload timer 0 Interval value.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”; the current value counter will pause. At least wait for 2*Tcylce, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.4.3.4 TMR0_INTV_VALUE_REG

偏移地址 : 0x0014			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	x	TMR0_INTV_VALUE. Timer 0 Interval Value. Note: the value setting should consider the system clock and the timer clock source.

3.4.3.5 TMR0_CUR_VALUE_REG

偏移地址 : 0x0018			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

3.4.3.6 TMR1_CTRL_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. 00: LOSC, 01: HOSC. 10: / 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is

			set to “0”; the current value counter will pause. At least wait for 2*Tcylce, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.4.3.7 TMR1_INTV_VALUE_REG

偏移地址 : 0x0024			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	x	TMR1_INTV_VALUE. Timer 1 Interval Value. Note: the value setting should consider the system clock and the timer clock source.

3.4.3.8 TMR1_CUR_VALUE_REG

偏移地址 : 0x0028			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

3.5 看门狗定时器(Watchdog)

3.5.1 概述

看门狗用于在控制器受到噪音和系统错误等故障干扰时恢复控制器的运行。本质上它是一个递减计数器，允许看门狗的时间长达16秒。它可以产生一个通用的复位或中断请求。

3.5.2 Watchdog 寄存器列表

模块名	**基地址**	
Timer	0x40040800	
寄存器名	**偏移地址**	**描述**
WDOG_IRQ_EN_REG	0x00A0	Watchdog Irq Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Irq Status Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register

WDOG_OUTPUT_CTRL_REG	0x00BC	Watchdog Output Control Register

3.5.3 Watchdog 寄存器描述

3.5.3.1 WDOG_IRQ_EN_REG

偏移地址 ：0x00A0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	WDOG_IRQ_EN 0: No effect 1: Watchdog interrupt enable

3.5.3.2 WDOG_IRQ_EN_REG

偏移地址 ：0x00A4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W	0x0	WDOG_IRQ_STA Watchdog irq pending. Write 1 to clear it 0: No effect 1: Pending, the interval value is reached.

3.5.3.3 WDOG_CTRL_REG

偏移地址 ：0x00B0			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:13	/	/	/
12:1	R/W	0x0	WDOG0_KEY_FIELD. Watchdog 0 Key Field. Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W	0x0	WDOG_RELOAD Watchdog Reload 0: no effect 1: reload the watchdog

3.5.3.4 WDOG_CFG_REG

偏移地址 ：0x00B4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
8	R/W	0x0	CLK_SEL 0: 32K 1: 32.768K
7:4	/	/	/
3:2	R/W	0x0	WDOG0_RST_CPU_MODE 00: when only reset CPU, watchdog resetn to CPU PORESETn. 01: when only reset CPU, watchdog resetn only to CPU SYSRESETn. 1x: when only reset CPU, watchdog resetn to CPU PORESETn/SYSRESETn.
1:0	R/W	0x1	WDOG0_CONFIG. 00: only reset CPU 01: reset whole system 10: only interrupt 11: /

3.5.3.5 WDOG_MODE_REG

偏移地址 ：0x00B8			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:4	R/W	0	WDOG_INTV_VALUE Watchdog Interval Value The watchdog clock source is HOSC/WDOG_PRESCALER. If the HOSC is turned off, the watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s)

			1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	W	0x0	WDOG_RST_110 When watchdog enable (WDOG_EN=1), written at value 3'b110. The watchdog reset should assert promptly. Other values are no valid.
0	R/W	0x0	WDOG_EN Watchdog Enable 0: no effect 1: Enable watchdog

3.5.3.6 WDOG_OUTPUT_CTRL_REG

偏移地址 : 0x00BC			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:5	/	/	/
4:0	R/W	0xA	WDOG_OUTPUT_CONTROL 0~31 the number of cycles with which the watch dog holds the reset signal

4 DMA 控制器

4.1 安全 DMA (SDMA)

4.1.1 概述

SDMA控制器有2个AHB DMA通道。并且按照优先级顺序排列，同一时刻只能有一个通道传输，高优先级通道传输完成后，低优先级通道传输才能开始。

SDMA控制器支持8位/16位/32位数据宽度。源端和目的端的数据宽度可以不同，但地址必须对齐。虽然SDMA的增加方式应该是地址对齐的，但它的字节计数器不可以是多个。即使SDMA已经启动，其源地址、目的地址、字节计数器寄存器仍可以被修改。

4.1.2 SDMA 寄存器列表

模块名	**基地址**	
SDMA Controller	0x40081000	
寄存器名	**偏移地址**	**描述**
SDMA_INT_CTRL_REG	0x0000	SDMA Interrupt Control Register
SDMA_INT_STA_REG	0x0004	SDMA Interrupt Status Register
SDMA_PTY_CFG_REG	0x0008	SDMA Priority Configure Register
SDMA_CTRL_REG	0x0100+N*0x20	Secure DMA Configuration (N=0,1)
SDMA_SRC_ADDR_REG	0x0100+N*0x20+0x4	Secure DMA Source Address (N=0,1)
SDMA_DEST_ADDR_REG	0x0100+N*0x20+0x8	Secure DMA Destination Address (N=0,1)
SDMA_BC_REG	0x0100+N*0x20+0xC	Secure DMA Byte Counter (N=0,1)

4.1.3 SDMA 寄存器描述

4.1.3.1 SDMA_IRQ_EN_REG

偏移地址 : 0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:4	/	/	/
3	R/W	0x0	SDMA1_END_IRQ_EN SDMA Channel 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.

2	R/W	0x0	SDMA1_HF_IRQ_EN SDMA Channel 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	SDMA0_END_IRQ_EN SDMA Channel 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	SDMA0_HF_IRQ_EN SDMA Channel 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

4.1.3.2 SDMA_IRQ_PEND_STA_REG

偏移地址 : 0x0004			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:4	/	/	/
3	R/W1C	0x0	SDMA1_END_IRQ_PEND. SDMA Channel 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
2	R/W1C	0x0	SDMA1_HF_IRQ_PEND. SDMA Channel 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W1C	0x0	SDMA0_END_IRQ_PEND. SDMA Channel 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W1C	0x0	SDMA0_HF_IRQ_PEND. SDMA Channel 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

4.1.3.3 SDMA_AUTO_GAT_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:17	/	/	/
16	R/W	0x0	SDMA Auto Clock Gating bit 0: SDMA auto clock gating enable 1: SDMA auto clock gating disable If SDMA works in continuous mode, this bit should be set to 1.
15:0	/	/	/

4.1.3.4 SDMA_CTRL_REG

偏移地址 ：0x100+N*0x20 (N=0,1)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	R/W	0x0	SDMA_LOADING. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will reset the corresponding DMA channel.
30	RO	0x0	DMA Busy Status. 0: DMA idle, 1: DMA busy.
29	R/W	0x0	SDMA_CONTI_MODE_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
28:26	R/W	0x0	SDMA Wait State. (n DMA clock cycles) 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128
25:24	R/W	0x0	SDMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit

			10: 32-bit 11: /
23	R/W	0x0	SDMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1, 01: 4
22	/	/	/
21	R/W	0x0	SDMA_DEST_ADDR_TYPE. DMA Destination Address Type. 0: Increment 1: No Change.
20:16	R/W	0x0	SDMA_DEST_DRQ_TYPE. DMA Destination DRQ Type. 00000 : SRAM 00001 : SPI0 TX 00010 : Reserved 00011 : UART0 TX 00100 : UART1 TX 00101 : SS TX 00110 : DAUDIO TX 00111 : FLASHC TX 01000 : Reserved 01001 : UART2 TX 01010 : AUDIO PWM 01011 : Reserved 01100 : Reserved others : /
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0: normal mode (the value read back is equal to the value that is written) 1: remain mode (the value read back is equal to the left bytes to be transferred).
14:10	/	/	/
9:8	R/W	0x0	SDMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /

7	R/W	0x0	SDMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: 4
6	/	/	/
5	R/W	0x0	SDMA_SRC_ADDR_TYPE. DMA Source Address Type. 0: Increment 1: No Change
4:0	R/W	0x0	SDMA_SRC_DRQ_TYPE. DMA Source DRQ Type. 00000 : SRAM 00001 : SPI0 RX 00010 : Reserved 00011 : UART0 RX 00100 : UART1 RX 00101 : SS RX 00110 : DAUDIO RX 00111 : FLASHC RX 01000 : Reserved 01001 : UART2 RX 01010 : Reserved 01011 : GPADC RX 01100 : Reserved others : /

4.1.3.5 SDMA_SRC_ADDR_REG

偏移地址 : 0x100+N*0x20+0x4 (N=0,1)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	SDMA_SRC_ADDR. DMA Channel N Source Address.(N=0,1)

4.1.3.6 SDMA_DEST_ADDR_REG

偏移地址 : 0x100+N*0x20+0x8 (N=0,1)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	SDMA_DEST_ADDR.

			DMA Channel N Destination Address.(N=0,1)

4.1.3.7 SDMA_BC_REG

偏移地址 ：0x100+N*0x20+0xC (N=0,1)		默认值: 0x0000_0000	
位置	**访问**	**默认值**	**描述**
31:18	/	/	/
17:0	R/W	0x0	SDMA_BC. DMA Channel N Byte Counter.(N=0,1) Note: If Byte Counter=0, DMA will transfer no byte. The maximum value is 128k.

4.2 非安全 DMA (NDMA)

4.2.1 概述

NDMA控制器有8个AHB DMA通道。并且按照优先级顺序排列，同一时刻只能同一时刻只能有一个通道传输，高优先级通道传输完成后，低优先级通道传输才能开始。

同SDMA类似，NDMA控制器也支持8位/16位/32位数据宽度。源端和目的端的数据宽度可以不同，但地址必须对齐。虽然NDMA的增加方式应该是地址对齐的，但它的字节计数器不可以是多个。即使NDMA已经启动，其源地址、目的地址、字节计数器寄存器仍可以被修改。

4.2.2 NDMA 寄存器列表

模块名	**基地址**	
NDMA Controller	0x40001000	
寄存器名	**偏移地址**	**描述**
NDMA_INT_CTRL_REG	0x0000	NDMA Interrupt Control Register
NDMA_INT_STA_REG	0x0004	NDMA Interrupt Status Register
NDMA_PTY_CFG_REG	0x0008	NDMA Priority Configure Register
NDMA_CTRL_REG	0x0100+N*0x20	Non-Secure DMA Configuration (N=0,1,2,3,4,5,6,7)
NDMA_SRC_ADDR_REG	0x0100+N*0x20+0x4	Non-Secure DMA Source Address (N=0,1,2,3,4,5,6,7)
NDMA_DEST_ADDR_REG	0x0100+N*0x20+0x8	Non-Secure DMA Destination Address (N=0,1,2,3,4,5,6,7)
NDMA_BC_REG	0x0100+N*0x20+0xC	Non-Secure DMA Byte Counter (N=0,1,2,3,4,5,6,7)

4.2.3 NDMA 寄存器描述

4.2.3.1 NDMA_IRQ_EN_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15	R/W	0x0	NDMA7_END_IRQ_EN. NDMA Channel 7 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
14	R/W	0x0	NDMA7_HF_IRQ_EN NDMA Channel 7 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	NDMA6_END_IRQ_EN NDMA Channel 6 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
12	R/W	0x0	NDMA6_HF_IRQ_EN NDMA Channel 6 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
11	R/W	0x0	NDMA5_END_IRQ_EN NDMA Channel 5 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
10	R/W	0x0	NDMA5_HF_IRQ_EN NDMA Channel 5 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	NDMA4_END_IRQ_EN NDMA Channel 4 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	NDMA4_HF_IRQ_EN NDMA Channel 4 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	R/W	0x0	NDMA3_END_IRQ_EN

			NDMA Channel 3 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
6	R/W	0x0	NDMA3_HF_IRQ_EN NDMA Channel 3 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	NDMA2_END_IRQ_EN NDMA Channel 2 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	NDMA2_HF_IRQ_EN NDMA Channel 2 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	R/W	0x0	NDMA1_END_IRQ_EN NDMA Channel 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
2	R/W	0x0	NDMA1_HF_IRQ_EN NDMA Channel 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	NDMA0_END_IRQ_EN NDMA Channel 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	NDMA0_HF_IRQ_EN NDMA Channel 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

4.2.3.2 NDMA_IRQ_PEND_STA_REG

偏移地址 : 0x0004			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15	R/W1C	0x0	NDMA7_END_IRQ_PEND. NDMA Channel 7 End Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.
14	R/W1C	0x0	NDMA7_HF_IRQ_PEND. NDMA Channel 7 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	NDMA6_END_IRQ_PEND. NDMA Channel 6 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
12	R/W1C	0x0	NDMA6_HF_IRQ_PEND. NDMA Channel 6 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	R/W1C	0x0	NDMA5_END_IRQ_PEND. NDMA Channel 5 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
10	R/W1C	0x0	NDMA5_HF_IRQ_PEND. NDMA Channel 5 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W1C	0x0	NDMA4_END_IRQ_PEND. NDMA Channel 4 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W1C	0x0	NDMA4_HF_IRQ_PEND. NDMA Channel 4 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	R/W1C	0x0	NDMA3_END_IRQ_PEND. NDMA Channel 3 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
6	R/W1C	0x0	NDMA3_HF_IRQ_PEND.

			NDMA Channel 3 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
5	R/W1C	0x0	NDMA2_END_IRQ_PEND. NDMA Channel 2 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
4	R/W1C	0x0	NDMA2_HF_IRQ_PEND. NDMA Channel 2 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
3	R/W1C	0x0	NDMA1_END_IRQ_PEND. NDMA Channel 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
2	R/W1C	0x0	NDMA1_HF_IRQ_PEND. NDMA Channel 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W1C	0x0	NDMA0_END_IRQ_PEND. NDMA Channel 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W1C	0x0	NDMA0_HF_IRQ_PEND. NDMA Channel 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

4.2.3.3 NDMA_AUTO_GAT_REG

偏移地址 : 0x0008			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:17	/	/	/
16	R/W	0x0	NDMA Auto Clock Gating bit 0: NDMA auto clock gating enable 1: NDMA auto clock gating disable

			If NDMA works in continuous mode, this bit should be set to 1.
15:0	/	/	/

4.2.3.4 NDMA_CTRL_REG

偏移地址 ：0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0x0	NDMA_LOADING. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will reset the corresponding DMA channel.
30	RO	0x0	DMA Busy Status. 0: DMA idle, 1: DMA busy.
29	R/W	0x0	NDMA_CONTI_MODE_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
28:26	R/W	0x0	NDMA Wait State. (n DMA clock cycles) 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128
25:24	R/W	0x0	NDMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
23	R/W	0x0	NDMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1, 01: 4
22	/	/	/
21	R/W	0x0	NDMA_DEST_ADDR_TYPE. DMA Destination Address Type.

			0: Increment 1: No Change.
20:16	R/W	0x0	NDMA_DEST_DRQ_TYPE. DMA Destination DRQ Type. 00000 : SRAM 00001 : SPI0 TX 00010 : Reserved 00011 : UART0 TX 00100 : UART1 TX 00101 : SS TX 00110 : DAUDIO TX 00111 : FLASHC TX 01000 : Reserved 01001 : UART2 TX 01010 : AUDIO PWM 01011 : Reserved 01100 : Reserved others : /
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0: normal mode (the value read back is equal to the value that is written) 1: remain mode (the value read back is equal to the left bytes to be transferred).
14:10	/	/	/.
9:8	R/W	0x0	NDMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
7	R/W	0x0	NDMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: 4
6	/	/	/
5	R/W	0x0	NDMA_SRC_ADDR_TYPE. DMA Source Address Type. 0: Increment 1: No Change

4:0	R/W	0x0	NDMA_SRC_DRQ_TYPE. DMA Source DRQ Type. 00000 : SRAM 00001 : SPI0 RX 00010 : Reserved 00011 : UART0 RX 00100 : UART1 RX 00101 : SS RX 00110 : DAUDIO RX 00111 : FLASHC RX 01000 : Reserved 01001 : UART2 RX 01010 : Reserved 01011 : GPADC RX 01100 : Reserved others : /

4.2.3.5 NDMA_SRC_ADDR_REG

偏移地址 : 0x100+N*0x20+0x4 (N=0,1,2,3,4,5,6,7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	NDMA_SRC_ADDR. DMA Channel N Source Address.(N=0,1,2,3,4,5,6,7)

4.2.3.6 NDMA_DEST_ADDR_REG

偏移地址 : 0x100+N*0x20+0x8 (N=0,1,2,3,4,5,6,7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	NDMA_DEST_ADDR. DMA Channel N Destination Address.(N=0,1,2,3,4,5,6,7)

4.2.3.7 NDMA_BC_REG

偏移地址 : 0x100+N*0x20+0xC (N=0,1,2,3,4,5,6,7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:18	/	/	/
17:0	R/W	0x0	NDMA_BC.

			DMA Channel N Byte Counter.(N=0,1,2,3,4,5,6,7) Note: If Byte Counter=0, DMA will transfer no byte. The maximum value is 128k.

5 安全模块

5.1 加解密算法加速器(Crypto Engine)

5.1.1 概述

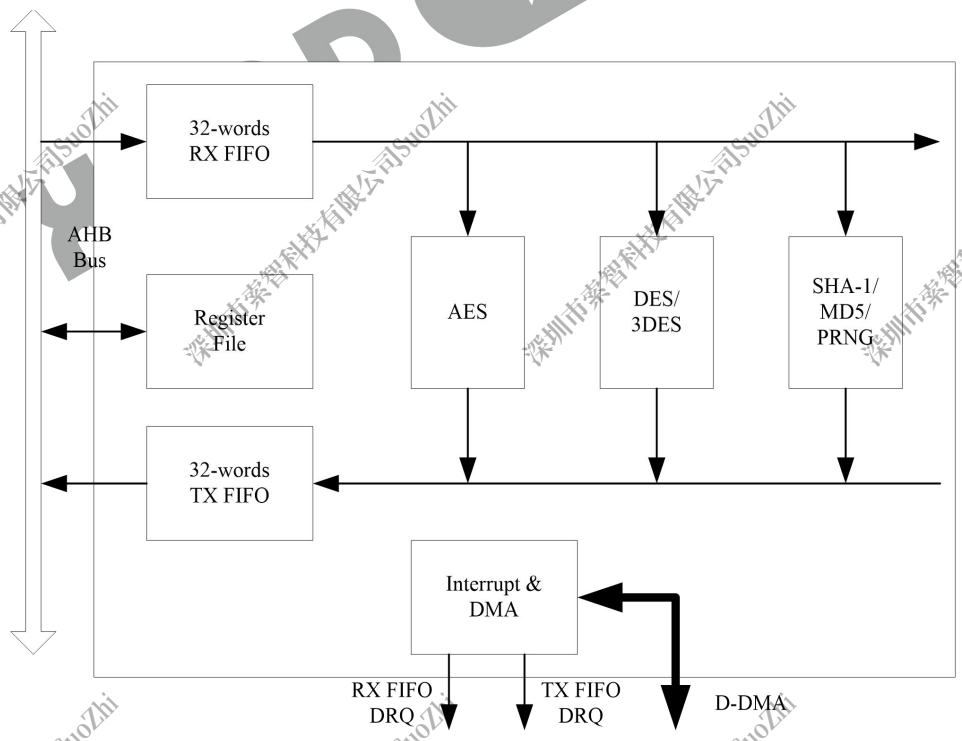
加密引擎(CE)是一种加密/解密算法加速器，它适用于各种应用场合，支持多种模式。不同的应用都支持CPU模式和DMA模式。

主要特性如下：

- 支持 AES、DES、3DES、SHA-1、MD5、PRNG、CRC32/16、SHA256；
- 支持 AES/DES/3DES 的 ECB, CBC, CTR 模式；
- 支持 AES 的 CTS 模式；
- 支持 128 位、192 位和 256 位 AES 密钥大小；
- 支持 160 位硬件 PRNG, 192 位种子；
- 用于高速应用的 32 字 RX FIFO 和 32 字 TX FIFO；
- 支持 CPU 模式和 DMA 模式；

CE模块的内部框架图如下图所示。

图 5-1 CE 模块内部框架图



5.1.2 Crypto Engine 寄存器列表

模块名	基地址	
Secure System Controller	0x40004000	
寄存器名	**偏移地址**	**描述**
CE_CTL_REG	0x00	CE Control Register
CE_KEY0_REG	0x04	Input Key 0/ PRNG Seed 0
CE_KEY1_REG	0x08	Input Key 1/ PRNG Seed 1
…	…	…
CE_KEY7_REG	0x20	Input Key 7
CE_IV0_REG	0x24	Initialization Vector 0
CE_IV1_REG	0x28	Initialization Vector 1
CE_IV2_REG	0x2C	Initialization Vector 2
CE_IV3_REG	0x30	Initialization Vector 3
CE_CNT0_REG	0x34	Counter 0/Initialization Vector 4
CE_CNT1_REG	0x38	Counter 1/Initialization Vector 5
CE_CNT2_REG	0x3C	Counter 2/Initialization Vector 6
CE_CNT3_REG	0x40	Counter 3/Initialization Vector 7
CE_FCSR_REG	0x44	FIFO Control/ Status Register
CE_ICSR_REG	0x48	Interrupt Control/ Status Register
CE_MD0_REG	0x4C	SHA1/MD5 Message Digest 0/PRNG Data0
CE_MD1_REG	0x50	SHA1/MD5 Message Digest 1/PRNG Data1
CE_MD2_REG	0x54	SHA1/MD5 Message Digest 2/PRNG Data2
CE_MD3_REG	0x58	SHA1/MD5 Message Digest 3/PRNG Data3
CE_MD4_REG	0x5C	SHA1/MD5 Message Digest 4/PRNG Data4
CE_CTS_LEN_REG	0x60	AES-CTS/CRC text length
CE_CRC_POLY_REG	0x70	CRC Poly Register
CRC_RESULT_REG	0x74	CRC Result Register
CE_MD5_REG	0xa0	SHA256 Message Digest Data 5

CE_MD6_REG	0xa4	SHA256 Message Digest Data 6
CE_MD7_REG	0xa8	SHA256 Message Digest Data 7
CE_RXFIFO_REG	0x200	RX FIFO input port
CE_TXFIFO_REG	0x204	TX FIFO output port

5.1.3 Crypto Engine 寄存器描述

5.1.3.1 CE_CTL_REG

偏移地址 ：0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R/W	0	CRC xor out value 0: CRC result as CRC out 1: CRC result xor 0xffffffff(CRC32) or 0xffff(CRC16) as CRC out
30	R/W	0	CRC ref out value 0: output word bit sequence not change 1: output word bit sequence reverse
29	R/W	0	CRC ref in value 0: input data bit sequence not change 1: input byte bit sequence reverse
28	R/W	0	CRC init value 0: init value is 0 1: init value is 0xffffffff for CRC32 or 0xffff for CRC16
27:24	R/W	0	KEY_SELECT AES/DES/3DES key select 0: Select input CE_KEYx (Normal Mode) 1: Select SID_RKEYx from SID 2: / 3-10: Select internal Key n (n from 0 to 7) Others: Reserved
18:16	R	x	DIE_ID Die Bonding ID
15	R/W	0	PRNG_MODE/CRC_CONT PRNG generator mode or CRC Package Continue 0: One-shot mode for PRNG or last package for CRC 1: Continue mode for PRNG or non-last package for CRC
14	R/W	0	IV_MODE IV mode for SHA-1/MD5 constants 0: use initial constants defined in FIPS-180

			1: use input IV
13:12	R/W	0	CE_OP_MODE CE Operation Mode 00: Electronic Code Book (ECB) mode 01: Cipher Block Chaining (CBC) mode 10: Counter (CTR) mode 11: Cipher Text Stealing (CTS) mode
11:10	R/W	0	CTR_WIDTH Counter Width for CTR Mode 00: 16-bits Counter 01: 32-bits Counter 10: 64-bits Counter 11: 128-bits Counter
9:8	R/W	0	AES_KEY_SIZE Key Size for AES 00: 128-bits 01: 192-bits 10: 256-bits 11: Reserved
7	R/W	0	CE_OP_DIR CE Operation Direction 0: Encryption 1: Decryption
6:4	R/W	0	CE_METHOD CE Method 000: AES 001: DES 010: Triple DES (3DES) 011: SHA-1 100: MD5 101: PRNG 110: SHA256 111: CRC
3	R/W	0	CRC_WIDTH 0: width 16, use 16 bits generate nominal 1: width 32, use 32 bits generate nominal
2	R/W	0	SHA1_SHA256_MD5_CRC_END_BIT SHA-1/MD5/SHA256/CRC Data End bit Write ‘1’ to tell SHA-1/MD5/SHA256/CRC engine that the text data ends. If RX FIFO is not empty, the engine would process the data in RX FIFO. After finishing message digest, this bit is clear to ‘0’ by

			hardware and message digest can be read out from digest registers. Notes: It is only used for SHA-1/MD5/SHA256/CRC engine.
1	R/W	0	PRNG_START PRNG start bit In PRNG one-shot mode, write ‘1’ to start PRNG. After generating one group random data (5 words), this bit is clear to ‘0’ by hardware.
0	R/W	0	CE_ENABLE CE Enable bit 0: Disable: write ‘0’ to tell engine ends 1: Enable: after configuration, set this bit to ‘1’ to start engine

5.1.3.2 CE_KEY[n]_REG

偏移地址 : 0x0004+N*4 (N=0,1,2,3,4,5,6,7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	CE_KEY Key[n] Input Value (n= 0~7)/ PRNG Seed[n] (n= 0~5)

5.1.3.3 CE_IV [n]_REG

偏移地址 : 0x0024+N*4 (N=0,1,2,3)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	CE_IV_VALUE Initialization Vector (IV[n]) Input Value (n= 0~3)

5.1.3.4 CE_CNT[n]_REG

偏移地址 : 0x0034+N*4 (N=0,1,2,3)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	CE_IV_VALUE Initialization Vector (IV[n]) Input Value (n= 0~3)

5.1.3.5 CE_FCSR_REG

偏移地址 : 0x0044			**默认值: 0x6000_0F0F**
位置	**访问**	**默认值**	**描述**
31	/	/	/

30	R	0x1	RXFIFO_STATUS RX FIFO Empty 0: No room for new word in RX FIFO 1: More than one room for new word in RX FIFO (>= 1 word)
29:24	R	0x20	RXFIFO_EMP_CNT RX FIFO Empty Space Word Counter
23	/	/	/
22	R	0	TXFIFO_STATUS TX FIFO Data Available Flag 0: No available data in TX FIFO 1: More than one data in TX FIFO (>= 1 word)
21:16	R	0	TXFIFO_AVA_CNT TX FIFO Available Word Counter
15:13	/	/	/
12:8	R/W	0xF	RXFIFO_INT_TRIG_LEVEL RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1 Notes: RX FIFO is used for input the data.
7:5	/	/	/
4:0	R/W	0xF	TXFIFO_INT_TRIG_LEVEL TX FIFO Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL + 1 Notes: TX FIFO is used for output the result data.

5.1.3.6 CE_ICSR_REG

偏移地址 : 0x0048			**默认值: 0x6000_0F0F**
位置	**访问**	**默认值**	**描述**
31:12	/	/	/
11	R/W	0	HASH_CRC_END_INT_PEND 0: No pending 1: HASH/CRC end pending
10	R/W	0	RXFIFO_EMP_PENDING_BIT RX FIFO Empty Pending bit 0: No pending 1: RX FIFO Empty pending Notes: Write ‘1’ to clear or automatic clear if interrupt condition

			fails.
9	/	/	/
8	R/W	0	TXFIFO_AVA_PENDING_BIT TX FIFO Data Available Pending bit 0: No TX FIFO pending 1: TX FIFO pending Notes: Write ‘1’ to clear or automatic clear if interrupt condition fails.
7:5	/	/	/
4	R/W	0	DRQ_ENABLE DRQ Enable 0: Disable DRQ (CPU polling mode) 1: Enable DRQ (DMA mode)
3	R/W	0	HASH_CRC_END_INT_ENABLE 0: Disable 1: Enable
2	R/W	0	RXFIFO_EMP_INT_ENABLE RX FIFO Empty Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when the number of empty room is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.
1	/	/	/
0	R/W	0	TXFIFO_AVA_INT_ENABLE TX FIFO Data Available Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when available data number is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.

5.1.3.7 CE_MD [n]_REG

偏移地址 : 0x004C+N*4 (N=0,1,2,3,4)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	AES-CTS / CRC text length in byte unit The value of '0' means no data.

5.1.3.8 CE_CTS_LEN_REG

偏移地址 ：0x0060			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R/W	0	AES-CTS / CRC text length in byte unit The value of '0' means no data.

5.1.3.9 CE_CRC_POLY_REG

偏移地址 ：0x0070			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R/W	0	CRC_POLY

5.1.3.10 CE_RESULT_REG

偏移地址 ：0x0070			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R/W	0	CRC computation result

5.1.3.11 CE_MD[n]_REG

偏移地址 ：0x00A0+(N-5)*4 (N=5,6,7)			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R	0	CE_SHA256_MDn SHA256 Message Digest n (n = 5~7)

5.1.3.12 CE_RX_REG

偏移地址 ：0x0200			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	W	0	CE_RX_FIFO 32-bits RX FIFO for Input

5.1.3.13 CE_TX_REG

偏移地址 ：0x0204			默认值: 0x0000_0000
位置	访问	默认值	描述
31:0	R	0	CE_TX_FIFO 32-bits TX FIFO for Output

5.1.4 CE 模块时钟要求

时钟名称	描述	要求
ahb_clk	AHB bus clock	>=24MHz
ss_clk	CE serial clock	<= 200MHz

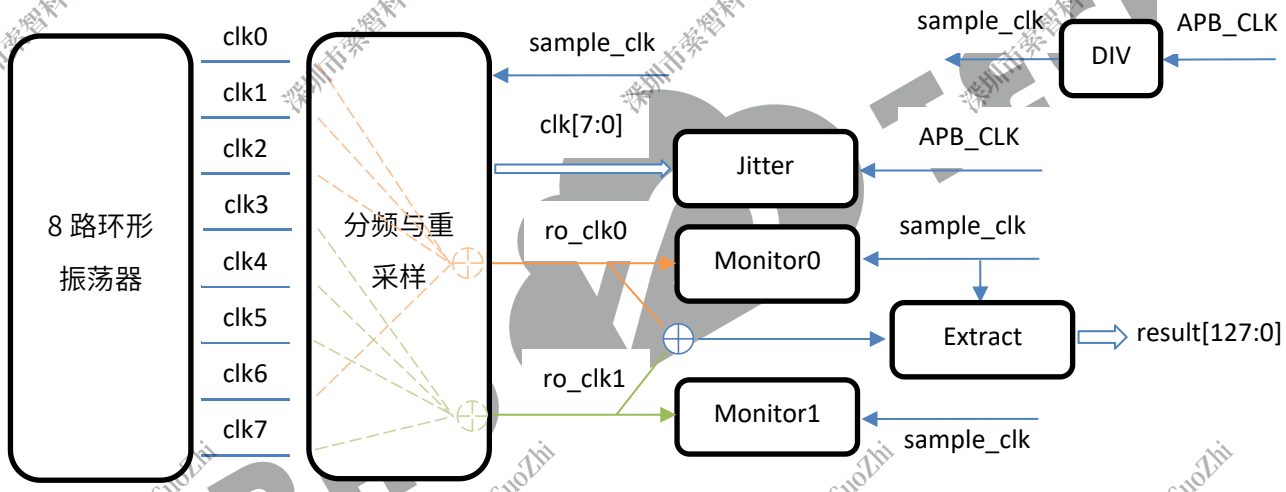
5.2 真随机数发生器(TRNG)

5.2.1 概述

TRNG(True Random Number Generator)是真随机数发生器，随机源是8路独立的环形振荡器，由模拟器件电源噪声产生频率抖动，用低频时钟重采样，然后进行弹性抽取和熵提取处理，最终输出128bit真随机数。

TRNG模块的数据流框架图如下图所示。

图 5- 2 TRNG 模块数据流框架图



- Jitter 模块是一个计数器模块，可以分别统计从环形振荡器送过来的 8 路时钟一段时间内的上升沿个数。其中计数时长 timing（REG 0x08）的单位时间长度取决于 APB 时钟（通常为 60MHz）。
- Monitor 模块是一个监测模块，功能是自动检测来自模拟的时钟是否符合要求。Monitor0 和 Monitor1 各监测 1 路时钟。特别说明，8 路时钟分成了两组，分别送给两个独立的监测模块，要想通过监测至少要 2 路起振。Monitor 有两个指标，分别是 RTC(游程长度)和 ATP(频数偏移)。
- RTC 是检测连续 0 和连续 1 的长度，超出阈值则报错，门限默认值 1032。
- ATP 是统计设定窗长(默认值 1024)内累计 0 和累计 1 的个数，超过阈值则报错，门限默认值 1009。
- Extract 模块是抽取模块，8 路时钟最终合成 1 路随机的 0/1 序列，在 Extract 模块中进行弹性抽取和熵提取处理，每次抽取输出一个 128bit 真随机数。

5.2.2 TRNG 寄存器列表

模块名	基地址
TRNG	0x40044400

寄存器名	偏移地址	描述
TRNG_CTRL_CFG_REG	0x0000	TRNG Control Register
TRNG_JITTER_CFG_REG	0x0004	TRNG Jitter Control Register
TRNG_JITTER_CNT_TIMING_REG	0x0008	TRNG Jitter Counter Timing Register
TRNG_MONITOR_RCT_REG	0x000C	TRNG Monitor RTC Register
TRNG_MONITOR_APT_REG	0x0010	TRNG Monitor APT Register
TRNG_EXTRACT_CFG_REG	0x0014	TRNG Extract Control Register
TRNG_RAND_BIT_URN0_REG	0x0018	TRNG Rand Data0 Register
TRNG_RAND_BIT_URN1_REG	0x001C	TRNG Rand Data1 Register
TRNG_RAND_BIT_URN2_REG	0x0020	TRNG Rand Data2 Register
TRNG_RAND_BIT_URN3_REG	0x0024	TRNG Rand Data3 Register
TRNG_JITTER_CNT_RESULT0_REG	0x0028	TRNG Jitter Counter Result0 Register
TRNG_JITTER_CNT_RESULT1_REG	0x002C	TRNG Jitter Counter Result1 Register
TRNG_JITTER_CNT_RESULT2_REG	0x0030	TRNG Jitter Counter Result2 Register
TRNG_JITTER_CNT_RESULT3_REG	0x0034	TRNG Jitter Counter Result3 Register
TRNG_JITTER_CNT_RESULT4_REG	0x0038	TRNG Jitter Counter Result4 Register
TRNG_JITTER_CNT_RESULT5_REG	0x003C	TRNG Jitter Counter Result5 Register
TRNG_JITTER_CNT_RESULT6_REG	0x0040	TRNG Jitter Counter Result6 Register
TRNG_JITTER_CNT_RESULT7_REG	0x0044	TRNG Jitter Counter Result7 Register
TRNG_JITTER_COUNTER_READY_REG	0x0048	TRNG Jitter Ready Register
TRNG_REG_ACCESS_CTR1	0x004C	TRNG Access Counter Low Register
TRNG_REG_ACCESS_CTR2	0x0050	TRNG Access Counter High Register

5.2.3 TRNG 寄存器描述

5.2.3.1 TRNG_CTL_REG

偏移地址 : 0x0000			默认值: 0x0000_0FF0
位置	访问	默认值	描述
31:15	/	/	/
14:12	R	0	TRNG_READY

			指示 TRNG 状态 4：表示两组 RO 全部 Failed 3：第一组 RO Failed 2：第二组 RO Failed 1：Busy 指示 0：IDLE 指示
11:4	R/W	0xFF	TRNG_RO_CTRL 按 Bit 分别对应 8 个环振的开启/关闭状态控制位，高有效
3	/	/	/
2:1	R/W	0	TURN_RO_DETUNE 微调 RO(环形振荡器)的振荡频率，值越大频率越快
0	R/W	0	TRNG_EN 0: Disable 1: Enable

5.2.3.2 TRNG_JITTER_REG

偏移地址 : 0x0004			**默认值: 0x0000_0002**
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R/W	0	TRNG_JITTER_COUNTER_START TRNG Jitter Counter 相关配置完成后，启动执行，上升沿有效
1	R/W	1	TRNG_COUNTER_2DIV 可选 2 分频器使能信号，高有效，默认高
0	R/W	0	TRNG_JITTER_WORK_EN 使能 Jitter 测量功能，同时控制 8 个分频器电路，高有效

5.2.3.3 TRNG_JITTER_CNT_TIMING_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:21	/	/	/
20:0	R	0x0	TRNG_JITTER_COUNTER_TIMING 定时器，用于计时给定时长

5.2.3.4 TRNG_MONITOR_RCT_REG

偏移地址 ：0x000C			默认值: 0x0000_0408
位置	**访问**	**默认值**	**描述**
31:12	/	/	/
11	R/W	0	TRNG_MONITOR_EN 检测使能信号，高电平有效且默认低
10:0	R/W	1032	TRNG_RCT_C RCT(游程长度)检测门限，默认值 1032。检测连续 0 或者 1 的长度，超出阈值则报错

5.2.3.5 TRNG_MONITOR_APT_REG

偏移地址 ：0x0010			默认值: 0x0040_03F1
位置	**访问**	**默认值**	**描述**
31:23	/	/	/
22:11	R/W	1024	TRNG_APT_W APT(频数偏移)检测窗长，默认值 1024。统计连续 trng_APT_W 个 Bit 中 0 和 1 的个数，任一个超过 trng_APT_C 则报错
10:0	R/W	1009	TRNG_APT_C APT(频数偏移)检测门限，默认值 1009

5.2.3.6 TRNG_EXSTRACT_CFG_REG

偏移地址 ：0x0014			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
25:12	R/W	0	TRNG_RESILIENT_RATIO 弹性抽取函数的抽取率
11:10	/	/	/
9	R/W1C	0	TRNG_EXTRACT_START 写 1 代表启动弹性抽取函数进行随机数生成，硬件自动清零
8	R/W	0	TRNG_RESILIENT_TYPE 熵提取方法 0: CRC32 1: 异或抽取
7:4	R/W	0	TRNG_RO_SAMPLING_RATION1 获取 trng_ro_sampling_clk 所需要的对主时钟 trng_clk 的再次分频倍数，实际生效分频值=trng_ro_sampling_div1+1
3:0	R/W	0	TRNG_RO_SAMPLING_RATION0 获取 trng_ro_sampling_clk 所需要的对主时钟 trng_clk 的首次分频倍数，实际生效分频值=trng_ro_sampling_div0+1

5.2.3.7 TRNG_RAND_BIT_URN0_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	RC	0	随机块内容，只读且读清零

5.2.3.8 TRNG_RAND_BIT_URN1_REG

偏移地址 ：0x001C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	RC	0	随机块内容，只读且读清零

5.2.3.9 TRNG_RAND_BIT_URN2_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	RC	0	随机块内容，只读且读清零

5.2.3.10 TRNG_RAND_BIT_URN3_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	RC	0	随机块内容，只读且读清零

5.2.3.11 TRNG_JITTER_CNT_RESULT0_REG

偏移地址 ：0x0028			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_COUNTER_RESULT0 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 0 路分频器输出的上升沿的个数

5.2.3.12 TRNG_JITTER_CNT_RESULT1_REG

偏移地址 ：0x002C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT1 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 1 路分频器输出的上升沿的个数

5.2.3.13 TRNG_JITTER_CNT_RESULT2_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT2 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 2 路分频器输出的上升沿的个数

5.2.3.14 TRNG_JITTER_CNT_RESULT3_REG

偏移地址 ：0x0034			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT3 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 3 路分频器输出的上升沿的个数

5.2.3.15 TRNG_JITTER_CNT_RESULT4_REG

偏移地址 ：0x0038			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT4 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 4 路分频器输出的上升沿的个数

5.2.3.16 TRNG_JITTER_CNT_RESULT5_REG

偏移地址 ：0x003C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT5 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 5 路分频器输出的上升沿的个数

5.2.3.17 TRNG_JITTER_CNT_RESULT6_REG

偏移地址 ：0x0040			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT6 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 6 路分频器输出的上升沿的个数

5.2.3.18 TRNG_JITTER_CNT_RESULT7_REG

偏移地址 ：0x0044			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	TRNG_JITTER_counter_RESULT7 在 TRNG_JITTER_COUNTER_TIMING 时间间隔内，第 7 路分频器输出的上升沿的个数

5.2.3.19 TRNG_JITTER_COUNTER_READY_REG

偏移地址 ：0x0048			默认值: 0x0000_0FF0
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R	0	TRNG_JITTER_READY 指示 TRNG JITTER 状态 1：READY 指示，可以取数 0：Busy/idle 状态

5.2.3.20 TRNG_REG_ACCESS_CTR1

偏移地址 ：0x004C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	x	统计 trng 寄存器被 APB 访问的次数（低 32 位），访问此寄存器不会增加次数，复位后无确定初值，休眠唤醒后此寄存器值会被保留

5.2.3.21 TRNG_REG_ACCESS_CTR2

偏移地址 ：0x0050			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R	x	统计 trng 寄存器被 APB 访问的次数（高 8 位），访问此寄存器不会增加次数，复位后无确定初值，休眠唤醒后此寄存器值会被保留

5.3 安全标识(Security ID)

5.3.1 概述

XR806包含1024位的eFuse空间，其中128位用于芯片ID，其他位为系统参数预留。Security ID的工作时钟为26MHz，来自APB时钟。

5.3.2 SID 寄存器列表

模块名	基地址	
Security ID	0x40043C00	
寄存器名	**偏移地址**	**描述**
SID_PRCTL_REG	0x0040	SID Program/Read Control Register
SID_PKEY_REG	0x0050	SID Program Key Value Register
SID_RKEY_REG	0x0060	SID Read Key Value Register
BURNED_TIMING_REG	0x0090	SID Burned Timing Control
SDI_DBG_REG	0x0094	SID Debug Register
SID_VALUE_REG	0x0100 – 0x01FF	SID Chip ID Register 0

5.3.3 SID 寄存器描述

5.3.3.1 SID_PR_CTRL_REG

偏移地址 : 0x0040			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:29	/	/	/
28	R/W	0	EFUSE_CLOCK_GATE_SW OSC40M（eFuse_clock）clock gate enable. When read or program the effuse, this bit should be set to 1
27:24	/	/	/
23:16	R/W	0	PG_INDEX Program Index The index value of 8-bits electrical fuse hardware macrocell address offset, and the lowest two bits must be zero.
15:8	R/W	0	OP_LOCK Operation Lock The Read Start Bit (bit1) and Program Start bit (bit0) and software one-short read start (bit4) only can be written when these bits

			(bit[15:8]) set to 0xAC
7:5	/	/	/
4	R/W	0	SW_ALL_READ_START Software one-short whole Efuse Read Start Write ‘1’ to start software whole Efuse Read and automatically clear to ‘0’ after read.
3	/	/	/
2	R	x	HW_READ_STATUS Hardware read status 0: No hardware operation 1: Hardware Reading
1	R/W	0	EFUSE_READ_START Software Read Start Write ‘1’ to start software read and automatically clear to ‘0’ after read.
0	R/W	0	EFUSE_PRG_START Software Program Start Write ‘1’ to start software program and automatically clear to ‘0’ after program.

5.3.3.2 SID_PKEY_REG

偏移地址 : 0x0050			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	SID_PGKEY_VALUE Program key value

5.3.3.3 SID_RKEY_REG

偏移地址 : 0x0060			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R	0	SID_RDKEY_VALUE Program key value

5.3.3.4 SID_BURN_TIMING_REG

偏移地址 ：0x0090			默认值: 0x630B_905C
位置	**访问**	**默认值**	**描述**
31:28	R/W	0x6	Control Taen of the eFuse Reading cycle value * Tosc Taen > Trd + 35ns
28:24	R/W	0x3	Control Trd of the eFuse Reading cycle value * Tosc Trd > 40ns
23:12	R/W	0X0B9	Control Taen of the eFuse program cycle value * Tosc Taen > Tpgm + 2300ns
11:0	R/W	0X05C	Control Tpgm of the eFuse Program cycle value * Tosc Tpgm >= 2300ns (2600ns > Tpgm > 2000ns)

5.3.3.5 SID_DBG_REG

偏移地址 ：0x0094			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:5	/	/	/
4	R/W	0	LDO-EFUSE software switch 0: soft switch off 1: soft switch on Note: Switch on accumulative total time should less than 1 second!!!
3:0	/	/	/

5.3.3.6 SID_VALUE_REG

偏移地址 ：0x0100~0x01FF			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	x	SID [32n+31: 32n]

6 外设及通用接口模块

6.1 外设安全控制(TZASC)

6.1.1 概述

TZASC 可以将总线外设、存储区域的访问权限灵活配置为安全访问或非安全访问。

6.1.2 TZASC 寄存器列表

模块名	基地址	
TZASC	0x4008A000	
寄存器名	**偏移地址**	**描述**
AHB_DEV_SEC_CTRL_REG	0x0000	The device on AHB bus secure control register
APB_DEV_SEC_CTRL_REG	0x0004	The device on APB bus secure control register
TZASC_INT_EN_REG	0x0008	TZASC secure case interrupt enable
TZASC_INT_STA_REG	0x000c	TZASC secure case interrupt pending
SEC_SPACE_ADRR_START_REG	0x0010+N*0x10	The secure space start address (N=0,1,2,3)
SEC_SPACE_ADRR_START_REG	0x0010+N*0x10+4	The secure space end address (N=0,1,2,3)
FLASHCTRL_SEC_CTRL_REG	0x0070	Flash controller secure space control register
FLASH_PSRAM_SEC_SPACE_ADRR_START_REG	0x0080+N*0x10	The secure space start address only for flash/psram storage address (N=0,1)
FLASH_PSRAM_SEC_SPACE_ADRR_END_REG	0x0080+N*0x10+4	The secure space end address only for flash/psram storage address (N=0,1)
TZASC_CLK_MANAGE_SEC_CASE_REG	0x00C0	The registers for clock manage secure control register

6.1.3 TZASC 寄存器描述

6.1.3.1 AHB_DEV_SEC_CTRL_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0x0	JTAG_FORCE_SEC_ENABLE Force JTAG connect enable in CPU secure state. It has high priority. 1: enable 0: disable
30:29	/	/	/
28	RW	0x0	WLAN_AHB_SEC 1: the device is secure 0: the device is no-secure
27	RW	0x0	BLE_SEC 1: the device is secure 0: the device is no-secure
26:22	/	/	/
21	RW	0x0	WLAN_CTRL_SEC 1: the device is secure 0: the device is no-secure
20	RW	0x0	SS_SEC 1: the device is secure 0: the device is no-secure
19	RW	0x0	SPI0_SEC 1: the device is secure 0: the device is no-secure
18	RW	0x0	SDC1_SEC 1: the device is secure 0: the device is no-secure
17	/	/	/
16	RW	0x0	SYSCTRL_SEC 1: the device is secure 0: the device is no-secure
15:14	/	/	/
13	RW	0x0	DCHACHE_CTRL_SEC 1: the device is secure 0: the device is no-secure

12	RW	0x0	FLASH_CTRL_SEC 1: the device is secure 0: the device is no-secure
11	RW	0x0	SRAM9_SEC 1: the device is secure 0: the device is no-secure
10	RW	0x0	SRAM08_SEC 1: the device is secure 0: the device is no-secure
9	RW	0x0	SRAM07_SEC 1: the device is secure 0: the device is no-secure
8	RW	0x0	SRAM06_SEC 1: the device is secure 0: the device is no-secure
7	RW	0x0	SRAM05_SEC 1: the device is secure 0: the device is no-secure
6	RW	0x0	SRAM04_SEC 1: the device is secure 0: the device is no-secure
5	RW	0x0	reserved
4	RW	0x0	SRAM03_SEC 1: the device is secure 0: the device is no-secure
3	RW	0x0	SRAM02_SEC 1: the device is secure 0: the device is no-secure
2	RW	0x0	SRAM01_SEC 1: the device is secure 0: the device is no-secure
1	RW	0x0	SRAM00_SEC 1: the device is secure 0: the device is no-secure
0	RW	0x0	ROM_SEC 1: the device is secure 0: the device is no-secure

6.1.3.2 APB_DEV_SEC_CTRL_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	/	/	/
30	RW	0x0	LPUART1_SEC 1: the device is secure 0: the device is no-secure
29			LPUART0_SEC 1: the device is secure 0: the device is no-secure
28:23	/	/	/
22	RW	0x0	CAPSEN_SEC 1: the device is secure 0: the device is no-secure
21	RW	0x0	FLASH_ENCRYPT_SEC 1: the device is secure 0: the device is no-secure
20	RW	0x0	ISO7816_SEC 1: the device is secure 0: the device is no-secure
19	RW	0x0	KEYSCAN_SEC 1: the device is secure 0: the device is no-secure
18	RW	0x0	TRNG_SEC 1: the device is secure 0: the device is no-secure
17	RW	0x0	CODEC_SEC 1: the device is secure 0: the device is no-secure
16	RW	0x0	UART2_SEC 1: the device is secure 0: the device is no-secure
15	RW	0x0	SID_SEC 1: the device is secure 0: the device is no-secure
14	RW	0x0	RTC_SEC 1: the device is secure

			0: the device is no-secure
13	RW	0x0	DMIC_SEC 1: the device is secure 0: the device is no-secure
12	RW	0x0	GPIO_SEC 1: the device is secure 0: the device is no-secure
11	RW	0x0	IRRX_SEC 1: the device is secure 0: the device is no-secure
10	RW	0x0	IRTX_SEC 1: the device is secure 0: the device is no-secure
9	RW	0x0	GPADC_SEC 1: the device is secure 0: the device is no-secure
8	RW	0x0	DAUDIO_SEC 1: the device is secure 0: the device is no-secure
7	RW	0x0	PWM_SEC 1: the device is secure 0: the device is no-secure
6	RW	0x0	TWI1_SEC 1: the device is secure 0: the device is no-secure
5	RW	0x0	TWI0_SEC 1: the device is secure 0: the device is no-secure
4	RW	0x0	UART1_SEC 1: the device is secure 0: the device is no-secure
3	RW	0x0	UART0_SEC 1: the device is secure 0: the device is no-secure
2	RW	0x0	TIMER_SEC 1: the device is secure 0: the device is no-secure
1	RW	0x0	CCM_SEC 1: the device is secure

			0: the device is no-secure
0	RW	0x0	GPRCM_SEC 1: the device is secure 0: the device is no-secure

6.1.3.3 TZASC_INT_EN_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	RW	0x0	TZASC_INT_EN TZASC Secure case occurred Interrupt Enable 0: Disable 1: Enable

6.1.3.4 TZASC_INT_STA_REG

偏移地址 ：0x000C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	RW	0x0	TZASC_INT_STA This bit is set if TZASC secure case has occurred. Writing 1 to this bit clears it. 0: TZASC secure case not occurred 1: TZASC secure case occurred

6.1.3.5 SEC_SPACE_ADRR_START_REG

偏移地址 ：0x10+N*0x10+0x0 (N=0,1,2,3)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	RW	0x0	SEC_SPACE_ADRR_START bit[31:2], The start word address of secure space.
1:0	/	/	/

6.1.3.6 SEC_SPACE_ADRR_END_REG

偏移地址 ：0x10+N*0x10+0x4 (N=0,1,2,3)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	SEC_SPACE_ADRR_END

			bit[31:2], The end word address of secure space.
1	/	/	/
0	RW	0x0	SEC_SPACE_VLD 0: invalid 1: the secure space is valid

6.1.3.7 FLASHCTRL_SEC_CTRL_REG

偏移地址 ：0x0070			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31	RW	0x0	FLASHCTRL_SEC_SPACE_ENABLE Enable flash controller secure space valid 0: disable 1: enable
30:28	/	/	/
27:16	RW	0x0	FLASHCTRL_SEC_SPACE_END_OFFSET_ADDR Bit[11:0], The end offset address of flash controller with secure space
15:12	/	/	/
11:0	RW	0x0	FLASHCTRL_SEC_SPACE_START_OFFSET_ADDR Bit[11:0], The start offset address of flash controller with secure space

6.1.3.8 FLASH_PSRAM_SEC_SPACE_ADRR_START_REG

偏移地址 ：0x80+N*0x10+0x0 (N=0,1)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	RW	0x0	FLASH_PSRAMSEC_SPACE_ADRR_START bit[31:2], The start word address of secure space.
1:0	/	/	/

6.1.3.9 FLASH_PSRAM_SEC_SPACE_ADRR_END_REG

偏移地址 ：0x80+N*0x10+0x4 (N=0,1)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	FLASH_PSRAM_SEC_SPACE_ADRR_END bit[31:2], The end word address of secure space.
1	RW	0x0	FLASH_PSRAM_SEL 0: the secure space for FLASH 1: the secure space for PSRAM

0	RW	0x0	FLASH_PSRAM_SEC_SPACE_VLD 0: invalid 1: the secure space is valid

6.1.3.10 TZASC_CLK_MANAGE_SEC_CASE_REG

偏移地址 : 0x00C0			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:5	/	/	/
6	RW	0x0	SYS_LFCLK_CTRL_SEC The Register SYS_LFCLK_CTRL (0x40040008) secure case 1: the register is secure 0: the register is no-secure
5	RW	0x0	DCXO_CTRL0_SEC The Register DCXO_CTRL0 (0x40040058) secure case 1: the register is secure 0: the register is no-secure
4	RW	0x0	PCLK_SPC_CLK_CTRL_SEC The Register PCLK_SPC_CLK_CTRL (0x4004045C) secure case 1: the register is secure 0: the register is no-secure
3	RW	0x0	CPU_BUS_CLKCFG_SEC The Register CPU_BUS_CLKCFG (0x40040400) secure case 1: the register is secure 0: the register is no-secure
2	RW	0x0	DEV_CLK_CTRL_SEC The Register DEV_CLK_CTRL (0x40040034) secure case 1: the register is secure 0: the register is no-secure
1	RW	0x0	SYS_CLK1_CTRL_SEC The Register SYS_CLK1_CTRL (0x40040024) secure case 1: the register is secure 0: the register is no-secure
0	RW	0x0	SYS_PLL_CTRL_SEC The Register SYS_PLL_CTRL (0x40040020) secure case 1: the register is secure 0: the register is no-secure

6.2 UART 接口

6.2.1 概述

UART用于与外设、调制解调器(数据载波设备，DCE)或数据集进行串行通信。数据从主设备(CPU)通过APB总线写到UART，它被转换成串行形式并传输到目标设备。串行数据也被UART接收并存储给主处理器(CPU)来读取。

UART包含用于控制字符长度、波特率、奇偶校验产生/检查和中断产生的寄存器。尽管来自UART的中断输出信号只有一个，但是有多个优先级的中断类型可以负责它的断言。每种中断类型都可以通过控制寄存器分别启用/禁用。

UART具有16450和16550操作模式，与一系列标准软件驱动程序兼容。在16550模式下，发送和接收操作都由FIFO缓冲。在16450模式下，这些FIFO被禁用。

UART支持从5到8位的字长度，一个可选的奇偶校验位和1、1½或2停止位，并完全由AMBA APB CPU接口控制。同时，包含一个16位可配置波特率发生器，一个8位临时寄存器，以及单独的发送和接收FIFO。并提供了8条调制解调器控制线和一个诊断环回模式。

中断可以产生自TX缓冲区/FIFO、 RX缓冲区/FIFO、调制解调器状态和线路状态条件等。

在需要红外SIR串行数据格式的系统中集成，UART可以配置为具有软件可编程的IrDA SIR模式。不选择该模式时，系统只提供UART (RS232标准)串口数据格式。

UART控制器包含以下特性：

- 兼容行业标准 16550 UARTs
- 64-Bytes 发送和接收数据 FIFO
- 支持 DMA 控制器接口
- 支持软硬件流制
- 支持 IrDA 1.0 SIR
- 支持 RS-485/9-bit 模式

下图描述了UART模块的典型时序。

图 6-1 UART 串行数据时序图

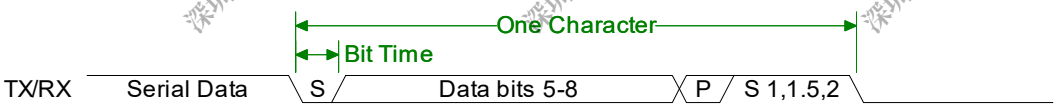
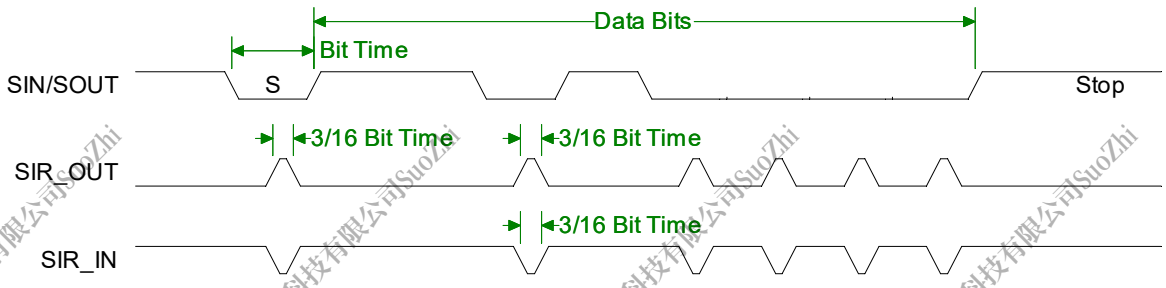


图 6-2 UART IrDA 时序图



6.2.2 UART 寄存器列表

模块名	基地址	
UART Controller 0	0x40040C00	
UART Controller 1	0x40041000	
UART Controller 2	0x40041400	
寄存器名	**偏移地址**	**描述**
UART_RBR_REG	0x0000	UART Receive Buffer Register
UART_THR_REG	0x0000	UART Transmit Holding Register
UART_DLL_REG	0x0000	UART Divisor Latch Low Register
UART_DLH_REG	0x0004	UART Divisor Latch High Register
UART_IER_REG	0x0004	UART Interrupt Enable Register
UART_IIR_REG	0x0008	UART Interrupt Identity Register
UART_FCR_REG	0x0008	UART FIFO Control Register
UART_LCR_REG	0x000C	UART Line Control Register
UART_MCR_REG	0x0010	UART Modem Control Register
UART_LSR_REG	0x0014	UART Line Status Register
UART_MSR_REG	0x0018	UART Modem Status Register
UART_SCH_REG	0x001C	UART Scratch Register
UART_USR_REG	0x007C	UART Status Register
UART_TFL_REG	0x0080	UART Transmit FIFO Level
UART_RFL_REG	0x0084	UART_RFL
UART_HALT_REG	0x00A4	UART Halt TX Register
UART_DBG_DLL_REG	0x00B0	UART Debug DLL Register
UART_DBG_DLH_REG	0x00B4	UART Debug DLH Register
UART_485_CTL_REG	0x00C0	UART RS485 Control and Status Register
RS485_ADDR_MATCH_REG	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHK_REG	0x00C8	UART RS485 Bus Idle Check Register
TX_DLY_REG	0x00CC	UART TX Delay Register
UART_BDCR_REG	0x00D4	UART Baudrate Detection Control Register

UART_BDCLR_REG	0x00D8	UART Baudrate Detection Counter Low Register
UART_BDCHR_REG	0x00DC	UART Baudrate Detection Counter High Register

6.2.3 UART 寄存器描述

6.2.3.1 UART_RBR_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR [0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

6.2.3.2 UART_THR_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

6.2.3.3 UART_DLL_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

6.2.3.4 UART_DLH_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

6.2.3.5 UART_IER_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	PTIME

			Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

6.2.3.6 UART_IIR_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

表 6- 1 UART 中断 ID 优先级

中断 ID	优先级	中断类型	中断源	中断复位
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/framing errors or break interrupt.	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address.	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled).	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout	No characters in or out of the RCVR FIFO during the last 4	Reading the receiver buffer

		indication	character times and there is at least 1character in it during this time.	register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

6.2.3.7 UART_FCR_REG

偏移地址 ：0x0008			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full

			11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enable, the TX DMA request will send when TFL is less than or equals to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the RX DRQ will send when RFL is equals to or more than FIFO Trigger Level. 1: Mode 1 In this mode, if TX FIFO is enabled and the PTE is high, the TX DMA request will send when TFL is less than or equals to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is empty. If RFL is equals to or more than FIFO Trigger Level, the RX DRQ will be set 1,in otherwise, it will be set 0.
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

6.2.3.8 UART_LCR_REG

偏移地址 : 0x000C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor

			Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is uset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 1,indicates that this is a address byte 10:9th bit = 0,indicates that this is a data byte Note: When use this function, PEN(LCR[3]) must set to 1.
3	R/W	0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Other/Wise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver checks only the first stop bit.

			0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

6.2.3.9 UART_MCR_REG

偏移地址 : 0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:6	R/W	0	UART_FUNCTION Select IrDA or RS485 0:Uart Mode 1:IrDA SIR Mode 2:RS485 Mode 3:Reverse
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the

			sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。 0：dtr_n de-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

6.2.3.10 UART_LSR_REG

偏移地址 ：0x0014			**默认值: 0x0000_0060**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.

6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	R	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error

			Reading the LSR clears the FE bit.
2	R	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	R	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is oveR/Written. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

6.2.3.11 UART_MSR_REG

偏移地址 ：0x0018			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has

			been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	R	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otheR/Wise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0	TERI Trailing Edge Ring Indicator

			This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otheR/Wise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otheR/Wise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

6.2.3.12 UART_SCH_REG

偏移地址 : 0x001C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

6.2.3.13 UART_USR_REG

偏移地址 ：0x007C			默认值: 0x0000_0006
位置	**访问**	**默认值**	**描述**
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

6.2.3.14 UART_TFL_REG

偏移地址 ：0x0080			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6:0	R	0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

6.2.3.15 UART_RFL_REG

偏移地址 ：0x0084			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6:0	R	0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

6.2.3.16 UART_RBR_REG

偏移地址 ：0x00A4			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	
7	R/W	0	DMA_PTE_RX RX_DRQ 的发送。 对于 DMA1 模式,当 RFL 大于等于 TRIG 或者接收超时发送 DRQ，否则 DRQ 为低。 对于 DMA0 模式,当 DMA_PTE_RX = 1 且 FIFO 开时，当 RFL 大于等于 TRIG 时发送 REQ，否则不发送。否则只要存在 RX 有效数据就发送 DRQ。
6	R/W	0	PTE TX_REQ 的发送。 对于 DMA1 模式 0(FIFO 开，FCR[3]=1),如果 PTE 信号为高，当 TFL 小于等于 TRIG，发送 DMA 请求。当 PTE 信号为低，当 FIFO 为空时发送 DMA 请求。DMA 请求只会在 FIFO 满的时候掉下来。

			对于 DMA0 模式(FIFO 关或 FCR[3]=0),如果 PTE 信号为高且 FIFO 开，当 TFL 小于等于 TRIG，发送 DMA 请求,如果条件不满足则 DRQ 掉下来。如果 PTE 信号为高且 FIFO 关，THRE 空时，发送 DMA 请求,如果条件不满足则 DRQ 掉下来。当 PTE 信号为低，当 FIFO 为空时发送 DMA 请求。
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0	CHANGE_UPDATE After the user using HALT[1] to change the baud rate or LCR configuration, write 1 to update the configuration and waiting this bit self-clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baud rate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled Note: If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

6.2.3.17 UART_TXDLY_REG

偏移地址 ：0x00CC			默认值: 0x0000_0000
位置	访问	默认值	描述
31:8	/	/	/
7:0	R/W	0	DLY The delay time between the last stop bit and the next start bit. The unit is Tclk. It is use to control the space between two bytes in TX.

6.2.3.18 UART_BDC_REG

偏移地址 ：0x00D4			默认值: 0x0000_0000
位置	访问	默认值	描述
31:2	/	/	/
1	R/W	0	Auto Baudrate Detect Enable 1: enable 0: disable Note: Set this bit to 1 to start the UART Baudrate Detection. The detection circuit will detect the start bit and count the cycles of PCLK in one bit duration. The number of the cycles will be written in the PCLK_NUM field. Set this bit to 0 to stop the UART Baudrate Detection.
0	R/W	0	Mode 1: Normal mode 0: Compare mode Note: In normal mode, when the detection circuit is enabled, the number of the PCLK cycles will be latched in each one bit duration and be written into the PCLK_NUM field. In compare mode, the number of the PCLK cycles will be latched in each one bit duration, but only the value which equals to the value latched in last time will be written into the PCLK_NUM field.

6.2.3.19 UART_BDCL_REG

偏移地址 ：0x00D8			默认值: 0x0000_0000
位置	访问	默认值	描述
31:8	/	/	/
7:0	R/W	0	PCLK_NUM_LOW

			The low 8 bits of the number of the cycles counted in one bit duration.

6.2.3.20 UART_ABCR_REG

偏移地址 ：0x00DC			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	PCLK_NUM_HIGH The high 8 bits of the number of the cycles counted in one bit duration.

6.3 LPUART 接口

6.3.1 概述

LPUART主要作用是用作系统休眠时，发特定字符或字符串组合唤醒系统，由于休眠时只能使用32K时钟源，最高波特率只支持到9600。

6.3.2 LPUART 寄存器列表

模块名	**基地址**	
LPUART0	0x40045800	
LPUART1	0x40045C00	
寄存器名	**偏移地址**	**描述**
LPUART_GP_SR_CON_REG	0x0000	LPUART Control Register
LPUART_BAUD_CONFIG_REG	0x0004	LPUART Baudrate Config Register
LPUART_RX_CONFIG_REG	0x0010	LPUART RX Config Register
LPUART_RX_DATA_REG	0x0014	LPUART RX Data Register
LPUART_INTR_EN_REG	0x0020	LPUART Interrupt Enable Register
LPUART_INTR_STATUS_REG	0x0024	LPUART Interrupt Status Register
LPUART_INTR_CLR_REG	0x0028	LPUART Interrupt Clear Register
LPUART_RX_CMP_REG1	0x002C	LPUART RX Compare Register1
LPUART_RX_CMP_REG2	0x0030	LPUART RX Compare Register2

6.3.3 LPUART 寄存器描述

6.3.3.1 LUART_GP_SR_CON_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8	W	1’b0	cfg_soft_rst_p 软复位。 软件置 1，硬件自清零。
7:0	/	/	/

6.3.3.2 LUART_BAUD_CONFIG_REG

偏移地址 ：0x0004			默认值: 0x0302_0006
位置	**访问**	**默认值**	**描述**
31:24	R/W	8’h03	cfg_denominator[7:0] 配置除数。由于采用双沿设计，如果时钟为 32K，目标波特率为 9600，则有 64K/9.6K=20/3=6 余 2，则该寄存器配 3。
23:16	R/W	8’h02	cfg_remainder[7:0] 配置余数。由于采用双沿设计，如果时钟为 32K，目标波特率为 9600，则有 64K/9.6K=20/3=6 余 2，则该寄存器配 2。
15:0	R/W	8’h06	cfg_quotient[15:0] 配置商值。由于采用双沿设计，如果时钟为 32K，目标波特率为 9600，则有 64K/9.6K=20/3=6 余 2，则该寄存器配 6。

6.3.3.3 LUART_RX_CONFIG_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:13	/	/	/
12	R/W	1’b0	cfg_rx_msb_first 1’b0: 先收取的作为 LSB 1’b1: 先收取的作为 MSB
11	/	/	/
10:8	R/W	3’h0	cfg_rx_data_width[2:0] 选择 RX 数据位的长度。

			3’b000: 4bit data 3’b001: 5bit data 3’b010: 6bit data 3’b011: 7bit data 3’b100: 8bit data 3’b101: 9bit data other: 8bit data 值得注意的是，RXFIFO 的位宽是 9bit，如果 rx data 少于 9bit，高位将被补零。
7	/	/	/
6:4	R/W	3’h0	cfg_rx_parity_mode[2:0] 选择 RX 校验位类型。 3’b000: 没有校验位。 3’b001: even。每个字节传送整个过程中 bit 为 1 的个数是偶数个。通过校验位来调整个数。 3’b010: odd。每个字节传送整个过程中 bit 为 1 的个数是奇 数。通过校验位来调整个数。 3’b011: space。即校验位总为 0。 3’b100: mark。即校验位总为 1。 3’b101/3’b110/3’b111: 没有校验位。
3	/	/	/
2	R	1’b0	rx_partiy_err_rpt 报告最近一次 RX 校验结果是否正确。 1’b0: 校验结果正确。 1’b1: 校验结果错误。
1	/	/	/
0	R/W	1’b0	cfg_rx_en 用于使能 RX。硬件在实现时，该信号被用作 RX 模块的时钟使能。 1’b1: enable RX 模块 1’b0: disable RX 模块

6.3.3.4 LUART_RX_DATA_REG

偏移地址 : 0x0014			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:9	/	/	/

8:0	R	9'h0	rx_data[8:0] 读取该寄存器将触发从 RXFIFO 读取新的数据。

6.3.3.5 LUART_INTR_EN_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:10	/	/	/
9	R/W	1'b0	cfg_rx_data_int_en 在非 RX FIFO 模式下，RX 接收到数据中断使能位。
8	/	/	/
7	R/W	1'b0	cfg_rx_data_cmp_int_en RX DATA Compare 中断使能位。
6:0	/	/	/

6.3.3.6 LUART_INTR_STATUS_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:10	/	/	/
9	R	1'b0	rx_data_int_flag 在非 RX FIFO 模式下，RX 接收到数据中断状态位。
8	/	/	/
7	R	1'b0	rx_data_cmp_int_flag RX DATA Compare 中断状态位。
6:0	/	/	/

6.3.3.7 LUART_INTR_CLR_REG

偏移地址 ：0x0028			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:10	/	/	/
9	W	1'b0	cfg_rx_data_int_clr 在非 RX FIFO 模式下，RX 接收到数据中断清零位。软件置位，硬件清零。
8	/	/	/

7	W	1'b0	cfg_rx_data_cmp_int_clr RX DATA Compare 中断清零位。软件置位，硬件清零。
6:0	/	/	/

6.3.3.8 LUART_RX_CMP_REG1

偏移地址 ：0x002C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:30	/	/	/
29:21	R/W	9'b0	cfg_rx_cmp2[8:0] 与 RX Data 进行第 3 个比较的寄存器。
20:12	R/W	9'b0	cfg_rx_cmp1[8:0] 与 RX Data 进行第 2 个比较的寄存器。
11:3	R/W	9'b0	cfg_rx_cmp0[8:0] 与 RX Data 进行第 1 个比较的寄存器。
2:0	R/W	3'b0	cfg_rx_cmp_num[2:0] 配置用于比较的个数。 0：比较 1 个数 1：比较 1 个数 2：比较 2 个数 3：比较 3 个数 4：比较 4 个数 5：比较 5 个数 6：比较 1 个数 7：比较 1 个数

6.3.3.9 LUART_RX_CMP_REG2

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:21	/	/	/
20:12	R/W	9'b0	cfg_rx_cmp4[8:0] 与 RX Data 进行第 5 个比较的寄存器。
11:3	R/W	9'b0	cfg_rx_cmp3[8:0] 与 RX Data 进行第 4 个比较的寄存器。

2:0	/	/	/

6.4 SPI 接口

6.4.1 概述

SPI支持4种不同的数据传输格式。软件可以通过设置SPI传输控制寄存器的bit1(极性)和bit0(相位)来选择SPI工作的四种模式之一。SPI控制器主程序使用SPI_SCLK信号来传输数据进出移位寄存器。使用四种可编程时钟相位和极性的任一组合，数据都可以被时钟采样。

在Phase 0, polar 0和Phase 1, polar 1操作期间，输出数据在时钟下降沿上变化，输入数据在时钟上升沿上移位。

在Phase 1, polar 0和Phase 0, polar 1操作期间，输出数据在时钟上升沿上变化，输入数据在时钟下降沿上移位。

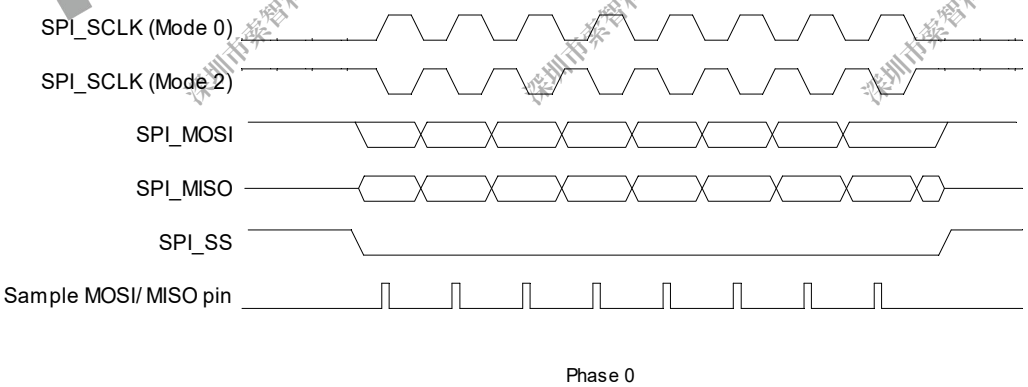
POL定义了SPI_SCLK处于空闲状态时的信号极性。当POL为'1'时SPI_SCLK为高电平，当POL为'0'时SPI_SCLK为低电平。PHA决定SPI_SCLK的前沿是用于数据建立还是采集。当PHA为'1'时，时钟沿用于数据建立，当PHA为'0'时，时钟沿用于数据采集。

下表给出了SPI四种模式的说明。

图 6- 3 SPI Modes with Clock Polarity and Phase

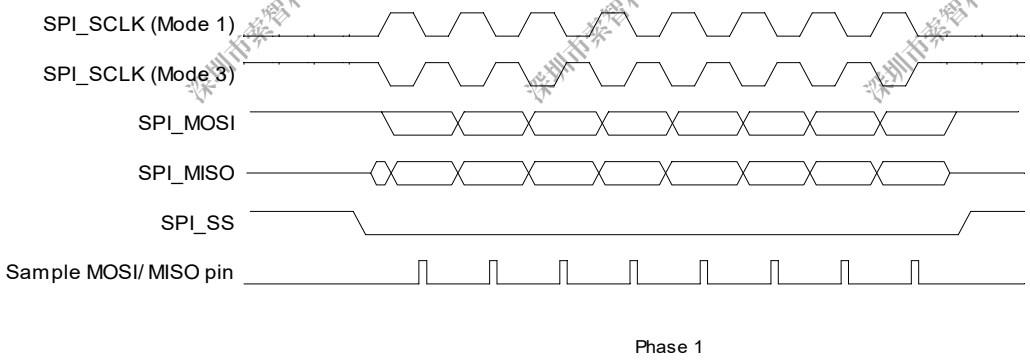
SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

图 6- 4 SPI Phase 0 Transfer Format



Phase 0

图 6- 5 SPI Phase 1 Transfer Format



6.4.2 SPI 寄存器列表

模块名	基地址	
SPI Controller 0	0x40005000	
寄存器名	**偏移地址**	**描述**
SPI_VER_REG	0x0000	SPI Version Number Register
SPI_CTRL_REG	0x0004	SPI Global Control Register
SPI_TCTRL_REG	0x0008	SPI Transfer Control register
SPI_IER_REG	0x0010	SPI Interrupt Control register
SPI_STA_REG	0x0014	SPI Interrupt Status register
SPI_FCTL_REG	0x0018	SPI FIFO Control register
SPI_FST_REG	0x001C	SPI FIFO Status register
SPI_WAIT_REG	0x0020	SPI Wait Clock Counter register
SPI_CCTR_REG	0x0024	SPI Clock Rate Control register
SPI_BC_REG	0x0030	SPI Burst Counter register
SPI_TC_REG	0x0034	SPI Transmit Counter Register
SPI_BCC_REG	0x0038	SPI Burst Control register
SPI_NDMA_MODE_CTRL_REG	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD_REG	0x0200	SPI TX Data register
SPI_RXD_REG	0x0300	SPI RX Data register

6.4.3 SPI 寄存器描述

6.4.3.1 SPI_VER_REG

偏移地址 ：0x0000			默认值: 0x0009_0000
位置	访问	默认值	描述
31:0	R	0x90000	SPI_VER

6.4.3.2 SPI_CTRL_REG

偏移地址 ：0x0004			默认值: 0x0000_0080
位置	访问	默认值	描述
31	R/WAC	0	SPI_RST SPI Software Reset Write 1 to this bit will clear the SPI controller, and auto clear to 0 when reset operation completes Write 0 has no effect.
30:8	/	/	/
7	R/W	1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: stop transmit data when RXFIFO full 0: normal operation Note: cannot be written when XCH=1
6:2	/	/	/
1	R/W	0	SPI_MODE Master Slave selection 0: slave mode 1: master mode Note: cannot be written when XCH=1
0	R/W	0	SPI_EN SPI Module Enable Control 0: SPI Controller Disable 1: SPI Controller Enable

6.4.3.3 SPI_TCTRL_REG

偏移地址 ：0x0008			默认值: 0x0000_0087
位置	**访问**	**默认值**	**描述**
31	R/W	0	XCH Exchange Burst In master mode it is used to start SPI burst. 0: Idle 1: Initiates exchange Write 1 to this bit will start the SPI burst and this bit will auto clear after finishing the bursts transfer specified by BC(Burst Counter). Write 1 to SPI_RST will also clear this bit. Write 0 to this bit has no effect.
30:15	/	/	/
14	R/W	0	SDDM Sending Data Delay Mode 0: normal sending 1: delay sending Set this bit to 1 to make the data that should be send with a delay of half cycle of SPI_CLK in dual io mode for SPI mode 0
13	R/W	0	SDM Master Sample Data Mode 1: normal sample mode 0: delay sample mode In normal sample mode, SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0	FBS First Transmit Bit Select 0: MSB first 1: LSB first
11	R/W	0	SDC Master Sample Data Control Set this bit to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed(>48MHz) read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave.

			0: normal operation, do not delay internal read sample point 1: delay internal read sample point
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note：Can’t be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Note：Can’t be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period(Burst Counter period) 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC(Transmit Counter). Note：Can’t be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_OWNER==1), set this bit to ‘1’ or ‘0’ to control the level of SS signal. 0: set SS to low 1: set SS to high Note：Can’t be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Note：Can’t be written when XCH=1.
5:4	R/W	0x0	SS_SEL

			SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Note：Can’t be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Note：Can’t be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note：Can’t be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note：Can’t be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Note：Can’t be written when XCH=1.

6.4.3.4 SPI_IER_REG

偏移地址 ：0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:14	R	0x0	Reserved.
13	R/W	0x0	SS_INT_EN

			SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	R	0x0	Reserved.
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable

4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	R	0x0	Reserved
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

6.4.3.5 SPI_STA_REG

偏移地址 : 0x0014			**默认值: 0x0000_0032**
位置	**访问**	**默认值**	**描述**
31:14	/	0x0	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF

			TXFIFO under run This bit is set when if the TXFIFO is under run. Writing 1 to this bit clears it. 0: TXFIFO is not under run 1: TXFIFO is under run
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Under run When set, this bit indicates that RXFIFO has under run. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL

			1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	reserved
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

6.4.3.6 SPI_FCTL_REG

偏移地址 : 0x0018			**默认值: 0x0040_0001**
位置	**访问**	**默认值**	**描述**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, write to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable Note: In normal mode, TX FIFO can only be read by SPI controller, write ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don’t set in normal

			operation and don’t set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, write ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable Note: In normal mode, RX FIFO can only be written by SPI controller, write ‘1’ to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don’t set in normal operation and don’t set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

6.4.3.7 SPI_FST_REG

偏移地址 : 0x001C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R	0x0	TB_WR

			TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	R	0x0	Reserved
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	R	0x0	Reserved
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

6.4.3.8 SPI_WAIT_REG

偏移地址 : 0x0020			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:20	/	/	/

19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Note：Can’t be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

6.4.3.9 SPI_CCTR_REG

偏移地址 : 0x0024			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0x0	CDR1 Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = SRC_CLK / 2^n.
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = SRC_CLK / (2*(n + 1)).

6.4.3.10 SPI_BC_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number . 0: 0 burst 1: 1 burst … N: N bursts

6.4.3.11 SPI_TC_REG

偏移地址 ：0x0034			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst . For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

6.4.3.12 SPI_BCC_REG

偏移地址 ：0x0038			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:29	R	0x0	Reserved
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode

			Note：Can’t be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don’t care by the device. 0: 0 burst 1: 1 burst … N: N bursts Note：Can’t be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Note：Can’t be written when XCH=1.

6.4.3.13 SPI_NDMA_MODE_CTRL_REG

偏移地址 : 0x0088			**默认值: 0x0000_00A5**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0xA5	NDMA_MODE_CTL 0xEA: NDMA handshake mode Note: NDMA wait mode doesn’t care this value. 0xA5 can be used in handshake mode, but 0xEA is better.

6.4.3.14 SPI_TXD_REG

偏移地址 : 0x0200			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	TDATA

			Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. Note: This address is writing-only if TF_TEST is ‘0’, and if TF_TEST is set to ‘1’, this address is readable and writable to test the TX FIFO through the AHB bus.

6.4.3.15 SPI_RXD_REG

偏移地址 : 0x0300			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. Note: This address is read-only if RF_TEST is ‘0’, and if RF_TEST is set to ‘1’, this address is readable and writable to test the RX FIFO through the AHB bus.

6.5 TWI 接口

6.5.1 概述

TWI控制器作为CPU主机与串行TWI总线之间的接口而设计。它可以支持所有标准的TWI传输，包括从设备和主设备。与TWI总线的通信是使用中断或轮询握手按字节进行的。TWI控制器可在标准模式(100K bps)或快速模式下工作，支持高达400K bps的数据速率。特定应用下支持多主和10位寻址模式。从模式下也支持通用呼叫寻址。

TWI控制器具有以下特性:

- 支持软件配置为从设备或主设备
- 支持重复 START 信号
- 支持多主系统
- 允许使用 TWI 总线进行 10 位寻址
- 执行仲裁和时钟同步
- 低地址和普通呼叫地址检测
- 在地址检测上中断
- 支持速度高达 400K bps（高速模式）

- 允许在宽范围的时钟输入频率内进行操作

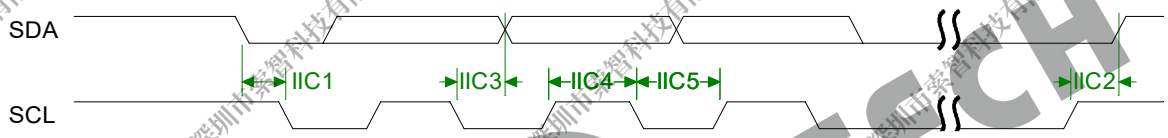
传输的数据总是以8位(字节)为单位，后面跟着一个确认位。每次传输可以传输的字节数是不受限制的。数据首先通过MSB串行传输。在数据传输的每个字节之间，接收设备将保持时钟线SCL低，迫使发送器进入等待状态，同时等待微处理器的响应。

数据传输必须有应答。除了每个字节之间的SCL保持之外，包括与应答相关的时钟周期在内，时钟线一直由主设备驱动。在每个字节发送后，发送器释放SDA线，以允许接收端拉低SDA线并发送一个应答信号(或将其保持高电平以发送一个“无应答”)给发送器。

当一个从端接收器不应答从端地址(因为没有资源可用而无法接收)时，数据线必须由从端保持高电平，这样主端就可以生成一个STOP条件来终止传输。从接收器也可以通过保持应答信号为高电平，以表示不期望在传输期间发送更多的数据。此时，主设备应该产生停止条件以中止转移。

下图说明了在TWI串行总线上SDA信号线和SCL信号线的关系。

图 6-6 TWI 时序图



6.5.2 TWI 寄存器列表

模块名	基地址	
TWI Controller 0	0x40041C00	
TWI Controller 1	0X40042000	
寄存器名	**偏移地址**	**描述**
TWI_ADDR_REG	0x0000	TWI Slave address
TWI_XADDR_REG	0x0004	TWI Extended slave address
TWI_DATA_REG	0x0008	TWI Data byte
TWI_CNTR_REG	0x000C	TWI Control register
TWI_STAT_REG	0x0010	TWI Status register
TWI_CCR_REG	0x0014	TWI Clock control register
TWI_SRST_REG	0x0018	TWI Software reset
TWI_EFR_REG	0x001C	TWI Enhance Feature register
TWI_LCR_REG	0x0020	TWI Line Control register

6.5.3 TWI 寄存器描述

6.5.3.1 TWI_ADDR_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:1	R/W	0	SLA Slave address - 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 - 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8] For 7-bit addressing: SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to ‘1’, the TWI will also recognize the general call address (00h). For 10-bit addressing: When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device’s extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

6.5.3.2 TWI_XADDR_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

6.5.3.3 TWI_DATA_REG

偏移地址 ：0x0008			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	TWI_DATA Data byte for transmitting or received

6.5.3.4 TWI_ADDR_REG

偏移地址 ：0x000C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1’ b0: The interrupt line always low 1’ b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN TWI Bus Enable 1’ b0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1’ b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to ‘1’
5	R/WAC	0	M_STA Master Mode Start When M_STA is set to ‘1’, TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to ‘1’ when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to ‘1’ when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a ‘0’ to this bit has no effect.

4	R/W1C	0	M_STP Master Mode Stop If M_STP is set to ‘1’ in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to ‘1’ in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a ‘0’ to this bit has no effect.
3	R/W1C	0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to ‘1’ when any of 28 (out of the possible 29) states is entered (see ‘STAT Register’ below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to ‘1’. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until ‘1’ is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0	A_ACK Assert Acknowledge When A_ACK is set to ‘1’, an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to ‘1’. 3. A data byte has been received in master or slave mode. When A_ACK is ‘0’, a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to ‘0’ in slave transmitter mode, the byte in the DATA register is assumed to be the ‘last byte’. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

6.5.3.5 TWI_STAT_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

6.5.3.6 TWI_CCR_REG

偏移地址 ：0x0014			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

6.5.3.7 TWI_SRST_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
0	R/W1C	0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

6.5.3.8 TWI_EFR_REG

偏移地址 ：0x001C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:2	/	/	/
0:1	R/W	0	DBN Data Byte number follow Read Command Control

			No Data Byte to be wrote after read command Only 1 byte data to be wrote after read command 2 bytes data can be wrote after read command 3 bytes data can be wrote after read command

6.5.3.9 TWI_LCR_REG

偏移地址 ：0x0020			默认值: 0x0000_003A
位置	**访问**	**默认值**	**描述**
31:6	/	/	/
5	R	1	SCL_STATE Current state of TWI_SCL 0 – low 1 - high
4	R	1	SDA_STATE Current state of TWI_SDA 0 – low 1 - high
3	R/W	1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level

			1 – output high level
0	R/W	0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

6.6 CIR 接口

6.6.1 概述

6.6.1.1 CIR 接收控制器（IRRX）

IRRX 包括以下特点:

- 全物理层实现
- 支持 CIR 远程控制
- 64x8 位 FIFO 数据缓冲区
- 可配置 FIFO 阈值

当在空中发现 CIR 信号时，CIR 接收机在可配置的频率下采样输入信号，并记录这些采样数据到 RX FIFO。CIR 接收机采用游程码(RLC)对脉冲宽度进行编码。编码数据在一个 64 级 8 位宽的 RX FIFO 缓冲，MSB 位用于记录接收 CIR 信号的极性。高电平表示为逻辑“1”，低电平表示为逻辑“0”。其余 7 位用于表示 RLC 的长度，最大长度为 128。如果一个电平(高电平或低电平)的持续周期超过 128，则再使用另一个字节。

在空气中，总是有一些噪音。可以通过设置一个阈值来滤除噪声，降低系统负荷，提高系统稳定性。

6.6.1.2 CIR 发射控制器（IRTX）

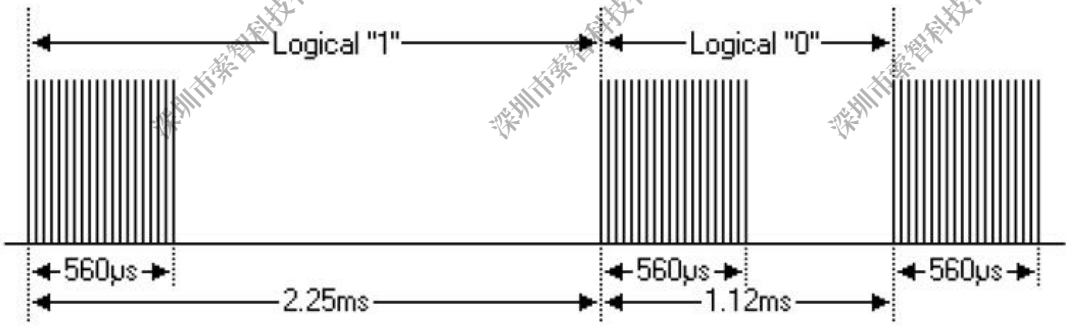
IRTX 包括以下特点:

- 支持工业标准 AMBA 外围总线(APB)，全兼容 AMBA 规范 2.0 修订版
- 全物理层实现
- 128 字节的 FIFO 数据缓冲区
- 可配置的载波频率
- 支持中断和 DMA 支持
- 支持 DMA 握手和等待模式

CIR 模式使用可变脉宽调制技术以实现远程控制应用下各种格式的红外编码。

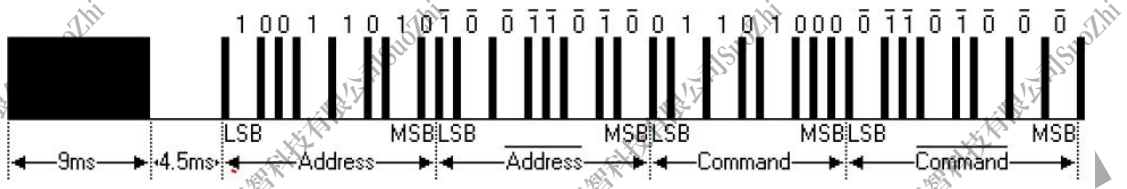
下图为 NEC 协议 IRTX 调制技术示例：逻辑“1”传输时间为 2.25ms，逻辑“0”传输时间为 1.12ms。

图 6- 7 IRTX 调制技术示例



下图为 IRTX NEC 协议示例。

图 6- 8 IRTX NEC 协议示例



6.6.2 CIR 寄存器列表

模块名	基地址	
CIR Receiver	0x40043800	
CIR Transmitter	0x40043400	
寄存器名	**偏移地址**	**描述**
CIR Receiver Register		
CIR_ACTL_REG	0x0000	CIR Active Control Register
CIR_CTL_REG	0x0004	CIR Control Register
CIR_RXCTL_REG	0x0010	CIR Receiver Configure Register
CIR_RXFIFO_REG	0x0020	CIR Receiver FIFO Register
CIR_RXINT_REG	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA_REG	0x0030	CIR Receiver Status Register
CIR_CONFIG_REG	0x0034	CIR Configure Register
CIR Transmitter Register		
CIR_TGLR_REG	0x0000	CIR Transmit Global Register
CIR_TMCR_REG	0x0004	CIR Transmit Modulation Control Register
CIR_TCR_REG	0x0008	CIR Transmit Control Register

CIR_IDC_H_REG	0x000C	CIR Transmit Idle Duration threshold Register
CIR_IDC_L_REG	0x0010	CIR Transmit Idle Duration threshold Register
CIR_TICR_H_REG	0x0014	CIR Transmit Idle Counter Register
CIR_TICR_L_REG	0x0018	CIR Transmit Idle Counter Register
CIR_TEL_REG	0x0020	CIR TX FIFO empty Level Register
CIR_TXINT_REG	0x0024	CIR Transmit Interrupt Control Register
CIR_TAC_REG	0x0028	CIR Transmit FIFO Available Counter Register
CIR_TXSTA_REG	0x002C	CIR Transmit Status Register
CIR_TXT_REG	0x0030	CIR Transmit Threshold Register
CIR_DMA_REG	0x0034	CIR DMA Control Register
CIR_TXFIFO_REG	0x0080	CIR Transmit FIFO Data Register

6.6.3 CIR Receiver 寄存器描述

6.6.3.1 CIR_CTL_REG

偏移地址 : 0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8	R/W	0x0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin 0: Low level 1: High level
7:6	R/W	0x0	Active Pulse Accept Mode 00: Start to accept data after detect de-bounce pulse edge 01: Start to accept data after detect de-bounce pulse edge 10: Start to accept data after detect low voltage de-bounce pulse 11: Start to accept data after detect high voltage de-bounce pulse
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable

			1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

6.6.3.2 CIR_RXCTL_REG

偏移地址 ：0x0010			默认值: 0x0000_0004
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

6.6.3.3 CIR_RXFIFO_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

6.6.3.4 CIR_RXINT_REG

偏移地址 ：0x002C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to ‘1’, the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.

4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to ‘1’, the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

6.6.3.5 CIR_RXSTA_REG

偏移地址 : 0x0030			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0x0 – Idle 0x1 – busy
6:5	/	/	/
4	R/W	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/

1	R/W	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

6.6.3.6 CIR_CONFIG_REG

偏移地址 : 0x0034			**默认值: 0x0000_1828**
位置	**访问**	**默认值**	**描述**
31:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0 –ATHR in Unit of (Sample Clock) 0x1 –ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enable, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR

			Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware. 0: all samples are recorded into RX FIFO 1: If the signal is only one sample duration, it is taken as noise and discarded. 2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded. … 61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.
1:0	R/W	0x0	SCS Sample Clock Select for CIR

SCS2	SCS[1]	SCS[0]	Sample Clock
0	0	0	ir_clk/64
0	0	1	ir_clk/128
0	1	0	ir_clk/256
0	1	1	ir_clk/512
1	0	0	ir_clk
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

6.6.4 CIR Transmit 寄存器描述

6.6.4.1 CIR_TGLR_REG

偏移地址 ：0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0	DRMC duty ratio of modulated carrier is high level /low level. 0: low level is the one time of high level 1: low level is the two times of high level 2: low level is the three times of high level 3: reserved

4:3	/	/	/
2	R/W	0	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
1	R/W	0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the TIC filed and CSS field will be clean during Transmit Reset. This field will automatically clean when the Transmit Reset is finished, and the CIR transmitter will state Idle .
0	R/W	0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

6.6.4.2 CIR_X_REG

偏移地址 : 0x0004			**默认值: 0x0000_009E**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of modulated carrier. Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK).The range of the modulated carrier is usually 30KHZ to 60KHz.The most consumer electronics is 38KHz. The default modulated carrier is 38KHz when FCLK is 6MHz. RFMC= FCLK/N.

6.6.4.3 CIR_TCR_REG

偏移地址 : 0x0008			**默认值: 0x0000_0002**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	CSS Cyclical Pulse Start/Stop Control Start to transmit when set to '1', 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start.
6:4	/	/	/
3:1	R/W	1	RCS Reference Clock Select for CIR Transmit(>=1)

			001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8 100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512
0	R/W	0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

6.6.4.4 CIR_IDC_H_REG

偏移地址 ：0x000C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
3:0	R/W	0	IDC_H Idle Duration Counter threshold(High 4 bit) Idle Duration = 128*IDC*Ts (IDC = 0~4095)

6.6.4.5 CIR_IDC_L_REG

偏移地址 ：0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	IDC_L Idle Duration Counter threshold(Low 8 bit) Idle Duration = 128*IDC*Ts (IDC = 0~4095)

6.6.4.6 CIR_TICR_H_REG

偏移地址 ：0x0014			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	TIC_H Transmit Idle Counter_H(High 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

6.6.4.7 CIR_TICR_L_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	TIC_L Transmit Idle Counter_L(Low 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reach the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

6.6.4.8 CIR_TEL_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

6.6.4.9 CIR_TXINT_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R/W	0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to ‘1’, the Tx FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less then the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0	TAI_EN TX FIFO Available Interrupt Enable 0:Disable 1:Enable
0	R/W	0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0:Disable 1:Enable

			TUI_EN Transmitter FIFO under run Interrupt Enable for Non-cyclical Pulse 0: Disable 1: Enable

6.6.4.10 CIR_TAC_REG

偏移地址 : 0x0028			**默认值: 0x0000_0128**
位置	**访问**	**默认值**	**描述**
31:6	/	/	/
7:0	R	128	TAC TX FIFO Available Space Counter 0: No available space in TX FIFO 1: 1 byte available space in TX FIFO 2: 2 byte available space in TX FIFO … 128: 128 byte available space in TX FIFO

6.6.4.11 CIR_TXSTA_REG

偏移地址 : 0x002C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:4	/	/	/
3	R	0	STCT Status of CIR Transmitter 0x0:Idle 0x1:Active This bit will automatically set when the controller begins transmit the data in the FIFO. The “1” will last when the data in the FIFO. It will automatically be cleaned to “0” when all data in the FIFO is transmitted. The bit is for debug.
2	R	0	DRQ DMA Request Flag When set to ‘1’, the Tx FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less then the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0	TAI TX FIFO Available Interrupt Flag

			0: TX FIFO not available by its level 1: TX FIFO available by its level This bit is cleared by writing a ‘1’.
0	R/W	0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a ‘1’.

6.6.4.12 CIR_TXT_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reach the Transmit Threshold set in this field.

6.6.4.13 CIR_DMA_CTL_REG

偏移地址 ：0x0034			默认值: 0x0000_00A5
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:6	R/W	2	00:dma_active is low 01:dma_active is high 10:dma_req 11:active is control by controller
5	R/W	1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	5	dma_active high after last signal is high

6.6.4.14 CIR_TXFIFO_REG

偏移地址 ：0x0080			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	W	0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number has been transmitted finished.

6.7 PWM 接口

6.7.1 概述

PWM模块带8个PWM通道，分4个PWM对：PWM01对、PWM23对、PWM45对、PWM67对，PWM01对由PWM0和PWM1通道构成，PWM23对由PWM2和PWM3通道构成，PWM45对由PWM4和PWM5通道构成，PWM67对由PWM6和PWM7通道构成。PWM对主要由3部分组成：1个时钟控制器、2个定时器逻辑模块、1个可编程死区发生器。

每个PWM通道支持PWM输出和捕捉输入两大功能。PWM通道的时钟源有24M_PLL和APB1（100M）可选，经过时钟控制器处理后送至PWM通道的定时器逻辑模块。PWM通道配置为PWM输出功能，其定时器逻辑模块可输出单脉冲波形或周期波形，频率范围在0Hz~24/100MHz之间。

PWM通道的定时器逻辑模块也可复用于捕捉输入功能，PWM通道捕捉到外部上升沿时锁存16-bit加法计数器当前值至上升沿锁存寄存器CRLR，PWM通道捕捉到外部下降沿时锁存16-bit加法计数器当前值至下降沿锁存寄存器CFLR，根据2个寄存器CRLR和CFLR的值可精确计算出外部时钟的频率。

PWM对可配置执行互补输出或插入死区时间的PWM波形对输出。当PWM对里的2个通道的prescale相同、period寄存器值相同且active state相反时，PWM对输出互补波形；当PWM对的可编程死区发生器被使能，PWM对输出插入死区时间的波形对，波形对的死区插入时间可控。

PWM通道配置为PWM输出功能或捕捉输入功能，PWM通道都可配置产生中断。配置为PWM输出功能时，每当16-bit加法计数器达到Entire cycle值，PWM通道可被使能产生中断；配置为捕捉输入功能时，每当PWM通道捕捉到外部上升沿，PWM通道可被使能产生1个中断，当PWM通道捕捉到下降沿，PWM通道可被使能产生1个中断，捕捉到上升沿或下降沿都可触发中断产生。

PWM控制器包含如下特性:

- 8 个 PWM 通道，分 4 个 PWM 对
- 支持脉冲、周期和互补对输出
- 支持捕捉输入
- 带可编程死区发生器，死区时间可控
- 0-24/100M 输出频率范围，0%-100%占空比可调，最小分辨率 1/65536
- 支持 PWM 输出和捕捉输入中断

6.7.2 PWM 寄存器列表

模块名	基地址	
PWM	0x40042800	
寄存器名	**偏移地址**	**描述**
PWM_PIER_REG	0x0000	PWM IRQ Enable Register
PWM_PISR_REG	0x0004	PWM IRQ Status Register
PWM_CIER_REG	0x0010	Capture IRQ Enable Register
PWM_CISR_REG	0x0014	Capture IRQ Status Register
PWM_PCCR01_REG	0x0020	PWM01 Clock Configuration Register
PWM_PCCR23_REG	0x0024	PWM23 Clock Configuration Register
PWM_PCCR45_REG	0x0028	PWM45 Clock Configuration Register
PWM_PCCR67_REG	0x002C	PWM67 Clock Configuration Register
PWM_PDZCR01_REG	0x0030	PWM01 Dead Zone Control Register
PWM_PDZCR23_REG	0x0034	PWM23 Dead Zone Control Register
PWM_PDZCR45_REG	0x0038	PWM45 Dead Zone Control Register
PWM_PDZCR67_REG	0x003C	PWM67 Dead Zone Control Register
PWM_PER_REG	0x0040	PWM Enable Register
PWM_CER_REG	0x0044	Capture Enable Register
PWM_PCR_REG	0x0060+0x0+N*0x20(N= 0~7)	PWM Control Register
PWM_PPR_REG	0x0060+0x4+N*0x20(N= 0~7)	PWM Period Register
PWM_PCNTR_REG	0x0060+0x8+N*0x20(N= 0~7)	PWM Count Register
PWM_CCR_REG	0x0060+0xC+N*0x20(N= 0~7)	Capture Control Register
PWM_CRLR_REG	0x0060+0x10+N*0x20(N= 0~7)	Capture Rise Lock Register
PWM_CFLR_REG	0x0060+0x14+N*0x20(N= 0~7)	Capture Fall Lock Register

6.7.3 PWM 寄存器描述

6.7.3.1 PWM_PIER_REG

偏移地址 ：0x0000			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0x0	PCIE7. PWM channel 7 Interrupt Enable. 0: PWM channel 7 Interrupt Disable; 1: PWM channel 7 Interrupt Enable.
6	R/W	0x0	PCIE6. PWM channel 6 Interrupt Enable. 0: PWM channel 6 Interrupt Disable; 1: PWM channel 6 Interrupt Enable.
5	R/W	0x0	PCIE5. PWM channel 5 Interrupt Enable. 0: PWM channel 5 Interrupt Disable; 1: PWM channel 5 Interrupt Enable.
4	R/W	0x0	PCIE4. PWM channel 4 Interrupt Enable. 0: PWM channel 4 Interrupt Disable; 1: PWM channel 4 Interrupt Enable.
3	R/W	0x0	PCIE3. PWM channel 3 Interrupt Enable. 0: PWM channel 3 Interrupt Disable; 1: PWM channel 3 Interrupt Enable.
2	R/W	0x0	PCIE2. PWM channel 2 Interrupt Enable. 0: PWM channel 2 Interrupt Disable; 1: PWM channel 2 Interrupt Enable.
1	R/W	0x0	PCIE1. PWM channel 1 Interrupt Enable. 0: PWM channel 1 Interrupt Disable; 1: PWM channel 1 Interrupt Enable.
0	R/W	0x0	PCIE0. PWM channel 0 Interrupt Enable. 0: PWM channel 0 Interrupt Disable; 1: PWM channel 0 Interrupt Enable.

6.7.3.2 PWM_PISR_REG

偏移地址 ：0x0004			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W1C	0x0	PIS7. PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. 1: PWM channel 7 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6. PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. 1: PWM channel 6 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5. PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. 1: PWM channel 5 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4. PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. 1: PWM channel 4 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3. PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. 1: PWM channel 3 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 3 interrupt status.

2	R/W1C	0x0	PIS2. PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. 1: PWM channel 2 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1. PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. 1: PWM channel 1 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0. PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. 1: PWM channel 0 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 0 interrupt status.

6.7.3.3 PWM_CIER_REG

偏移地址 : 0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15	R/W	0x0	CFIE7. If this enable bit is set 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock Interrupt disable; 1: Capture channel 7 fall lock Interrupt enable.
14	R/W	0x0	CRIE7. If this enable bit is set 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock Interrupt disable; 1: Capture channel 7 rise lock Interrupt enable.
13	R/W	0x0	CFIE6. If this enable bit is set 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock Interrupt disable;

			1: Capture channel 6 fall lock Interrupt enable.
12	R/W	0x0	CRIE6. If this enable bit is set 1, when capture channel 6 captures rising edge, it generates a capture channel 6 pending. 0: Capture channel 6 rise lock Interrupt disable; 1: Capture channel 6 rise lock Interrupt enable.
11	R/W	0x0	CFIE5. If this enable bit is set 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock Interrupt disable; 1: Capture channel 5 fall lock Interrupt enable.
10	R/W	0x0	CRIE5. If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
9	R/W	0x0	CFIE4. If this enable bit is set 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock Interrupt disable; 1: Capture channel 4 fall lock Interrupt enable.
8	R/W	0x0	CRIE4. If this enable bit is set 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock Interrupt disable; 1: Capture channel 4 rise lock Interrupt enable.
7	R/W	0x0	CFIE3. If this enable bit is set 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock Interrupt disable; 1: Capture channel 3 fall lock Interrupt enable.
6	R/W	0x0	CRIE3. If this enable bit is set 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock Interrupt disable; 1: Capture channel 3 rise lock Interrupt enable.
5	R/W	0x0	CFIE2. If this enable bit is set 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock Interrupt disable; 1: Capture channel 2 fall lock Interrupt enable.
4	R/W	0x0	CRIE2. If this enable bit is set 1, when capture channel 2 captures rising edge,

			it generates a capture channel 2 pending. 0: Capture channel 2 rise lock Interrupt disable; 1: Capture channel 2 rise lock Interrupt enable.
3	R/W	0x0	CFIE1. If this enable bit is set 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending. 0: Capture channel 1 fall lock Interrupt disable; 1: Capture channel 1 fall lock Interrupt enable.
2	R/W	0x0	CRIE1. If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable; 1: Capture channel 1 rise lock Interrupt enable.
1	R/W	0x0	CFIE0. If this enable bit is set 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock Interrupt disable; 1: Capture channel 0 fall lock Interrupt enable.
0	R/W	0x0	CRIE0. If this enable bit is set 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending. 0: Capture channel 0 rise lock Interrupt disable; 1: Capture channel 0 rise lock Interrupt enable.

6.7.3.4 PWM_CISR_REG

偏移地址 : 0x0014			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
15	R/W1C	0x0	CFIS7. Capture channel 7 falling lock interrupt status. When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7. Capture channel 7 rising lock interrupt status. When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit.

			Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6. Capture channel 6 falling lock interrupt status. When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
12	R/W1C	0x0	CRIS6. Capture channel 6 rising lock interrupt status. When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5. Capture channel 5 falling lock interrupt status. When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	CRIS5. Capture channel 5 rising lock interrupt status. When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	CFIS4. Capture channel 4 falling lock interrupt status. When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set 1 by hardware.

			Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	CRIS4. Capture channel 4 rising lock interrupt status. When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
7	R/W1C	0x0	CFIS3. Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (CFIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3. Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (CRIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2. Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (CFIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2. Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2

			rise lock interrupt (CRIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1. Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (CFIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1. Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (CRIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0. Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (CFIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0. Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (CRIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.

6.7.3.5 PWM_PCCR01_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8:7	R/W	0x0	PWM01_CLK_SRC. Select PWM01 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM1. Bypass PWM01 clock source to PWM1 output. 0: not bypass 1: bypass
5	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM0. Bypass PWM01 clock source to PWM0 output. 0: not bypass 1: bypass
4	R/W	0x0	PWM01_CLK_GATING. Gating clock for PWM01. 0: Mask 1: Pass
0:3	R/W	0x0	PWM01_CLK_DIV_M. PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

6.7.3.6 PWM_PCCR23_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:9	/	/	/

8:7	R/W	0x0	PWM23_CLK_SRC_SEL. Select PWM23 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM3. Bypass PWM23 clock source to PWM3 output. 0: not bypass 1: bypass
5	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM2. Bypass PWM23 clock source to PWM2 output. 0: not bypass 1: bypass
4	R/W	0x0	PWM23_CLK_GATING Gating clock for PWM23. 0: Mask 1: Pass
0:3	R/W	0x0	PWM23_CLK_DIV_M. PWM23 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

6.7.3.7 PWM_PCCR45_REG

偏移地址 : 0x0028			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8:7	R/W	0x0	PWM45_CLK_SRC_SEL. Select PWM45 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM5.

			Bypass PWM45 clock source to PWM5 output. 0: not bypass 1: bypass
5	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM4. Bypass PWM45 clock source to PWM4 output. 0: not bypass 1: bypass
4	R/W	0x0	PWM45_CLK_GATING. Gating clock for PWM45. 0: Mask 1: Pass
0:3	R/W	0x0	PWM45_CLK_DIV_M. PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

6.7.3.8 PWM_PCCR67_REG

偏移地址 ：0x002C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL. Select PWM67 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM7. Bypass PWM67 clock source to PWM7 output. 0: not bypass 1: bypass
5	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM6. Bypass PWM67 clock source to PWM6 output. 0: not bypass

			1: bypass
4	R/W	0x0	PWM67_CLK_GATING. Gating clock for PWM67. 0: Mask 1: Pass
0:3	R/W	0x0	PWM67_CLK_DIV_M. PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

6.7.3.9 PWM_PDZCR01_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
15:8	R/W	0x0	PDZINTV01. PWM01 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN. PWM01 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

6.7.3.10 PWM_PDZCR23_REG

偏移地址 ：0x0034			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
15:8	R/W	0x0	PWM23_DZ_INTV. PWM23 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN. PWM23 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

6.7.3.11 PWM_PDZCR45_REG

偏移地址 ：0x0038			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
15:8	R/W	0x0	PWM45_DZ_INTV. PWM45 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN. PWM45 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

6.7.3.12 PWM_PDZCR67_REG

偏移地址 ：0x003C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
15:8	R/W	0x0	PWM67_DZ_INTV. PWM67 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN. PWM67 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

6.7.3.13 PWM_PER_REG

偏移地址 ：0x0040			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:1	/	/	/
7	R/W	0x0	PWM7_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel7 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
6	R/W	0x0	PWM6_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel6 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
5	R/W	0x0	PWM5_EN. When enable PWM, the 16-bit up-counter starts working and PWM

			channel5 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
4	R/W	0x0	PWM4_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel4 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
3	R/W	0x0	PWM3_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel3 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
2	R/W	0x0	PWM2_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel2 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
1	R/W	0x0	PWM1_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel1 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
0	R/W	0x0	PWM0_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel0 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.

6.7.3.14 PWM_CER_REG

偏移地址 : 0x0044			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0x0	CAP7_EN. When enable capture function, the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
6	R/W	0x0	CAP6_EN. When enable capture function, the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge.

			0: Capture disable 1: Capture enable.
5	R/W	0x0	CAP5_EN. When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
4	R/W	0x0	CAP4_EN. When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
3	R/W	0x0	CAP3_EN. When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
2	R/W	0x0	CAP2_EN. When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
1	R/W	0x0	CAP1_EN. When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
0	R/W	0x0	CAP0_EN. When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

6.7.3.15 PWM_PCR_REG

偏移地址 : 0x60+0x0+N*0x20 (N= 0~7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:13	/	/	/

11	R	0x0	PWM_PERIOD_RDY. PWM period register ready. 0: PWM period register is ready to write 1: PWM period register is busy.
10	R/W1S	0x0	PWM_PUL_START. PWM pulse output start. 0: no effect 1: output 1 pulse. After finishing configurating for outputting pulse, set this bit once and then PWM would output one pulse. After the pulse is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE. PWM output mode select. 0: cycle mode 1: pulse mode.
8	R/W	0x0	PWM_ACT_STA. PWM active state. 0: Low Level 1: High Level.
7:0	R/W	0x00	PWM_PRESCAL_K. PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256.

6.7.3.16 PWM_PPR_REG

偏移地址 :0x60+0x4+N*0x20 (N= 0~7)		**默认值: 0x0000_0000**	
位置	**访问**	**默认值**	**描述**
31:16	R/W	0x0000	PWM_ENTIRE_CYCLE. Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK.
15:0	R/W	0x0000	PWM _ACT_CYCLE.

			Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

6.7.3.17 PWM_PCNTR_REG

偏移地址 :0x60+0x8+N*0x20 (N= 0~7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15:0	R	0x0000	On PWM output or capture input, reading this register could get the current value of the PWM 16bit up-counter.

6.7.3.18 PWM_CCR_REG

偏移地址 : 0x60+0xC+N*0x20 (N= 0~7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:3	/	/	/
2	R/W	0x0	CRLF. When capture channel captures rising edge, the 16-bit up-counter’s current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
1	R/W	0x0	CFLF. When capture channel captures falling edge, the 16-bit up-counter’s current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
0	R/W	0x0	CAPINV. Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: not inverse 1: inverse

6.7.3.19 PWM_CRLR_REG

偏移地址 : 0x60+0x10+N*0x20 (N= 0~7)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:16	/	/	/

15:0	R	0x0000	When capture channel captures rising edge, the 16-bit up-counter’ s current value is latched to this register.

6.7.3.20 PWM_CFLR_REG

偏移地址 ：0x60+0x14+N*0x20 (N= 0~7)			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	/	/	/
15:0	R	0x0000	When capture channel captures falling edge, the 16-bit up-counter’ s current value is latched to this register.

6.8 智能卡接口(ISO7816)

6.8.1 概述

智能卡读卡器(SCR)是在系统和智能卡之间传输数据的通信控制器。控制器可以执行完整的智能卡会话，包括卡激活、卡去激活、冷/热复位、应答复位(ATR)响应接收、数据传输等。

主要特性如下:

- 支持 ISO/IEC 7816-3:1997(E)和 EMV2000(4.0)规范
- 执行完整智能卡会话所需的功能，包括:
  - 卡片激活和去激活
  - 冷/热复位
  - 应答复位(ATR)响应接收
  - 数据传输
- 支持可调时钟速率和比特率
- 可配置的自动字节重复
- 支持常用的通信协议
  - T=0，异步半双工字符传输
  - T=1，异步半双工块传输
- 128 位 FIFO 用于数据发送和接收。
- 支持 FIFO 带阈值的接收和传输缓冲区(高达 128 位)
- 支持可配置的定时功能
  - 智能卡启动时间
  - 智能卡复位时间
  - 保护时间
  - 超时计时器

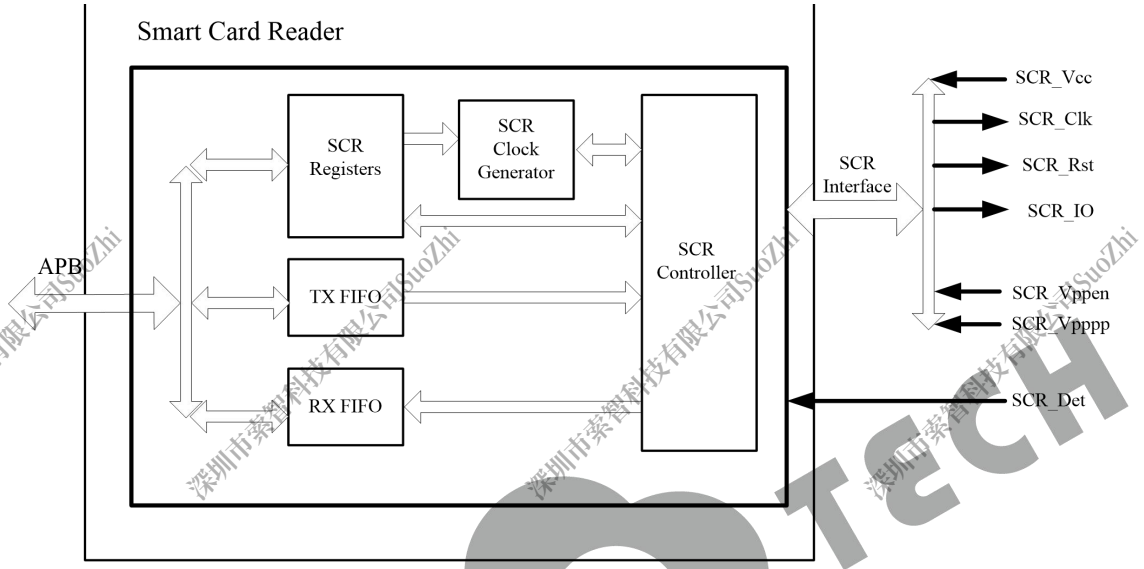
- 支持同步和任何其他非 ISO 7816 和非 EMV 卡

6.8.2 功能描述

6.8.2.1 模块框图

SCR逻辑框图如下图所示。

图 6- 9 SCR 逻辑框图



6.8.2.2 接口信号

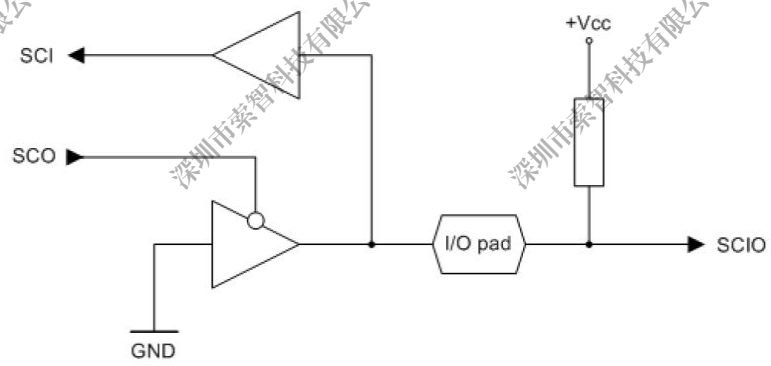
SCR 的接口信号如下表所示。

表 6- 2 SCR 接口信号

信号名称	描述	类型
SCR_CLK	Clock of SCR	O
SCR_RST	Reset signal	O
SCR_IO	Data signal	I/O
SCR_DET	Card detect signal	I
SCR_PWREN	Smart card power enable	O
SCR_VPPEN	Smart card program power enable	O
SCR_VPPPP	Smart Card Vpp Pause and Prog	O

6.8.2.3 管脚应用电路

图 6- 10 SCR IO Pad 框图



注意

SCIO 管脚需要接上拉电阻。

6.8.2.4 电气特性

6.8.2.5 SCR 冷复位

图 6-11 SCR 冷复位时序框图

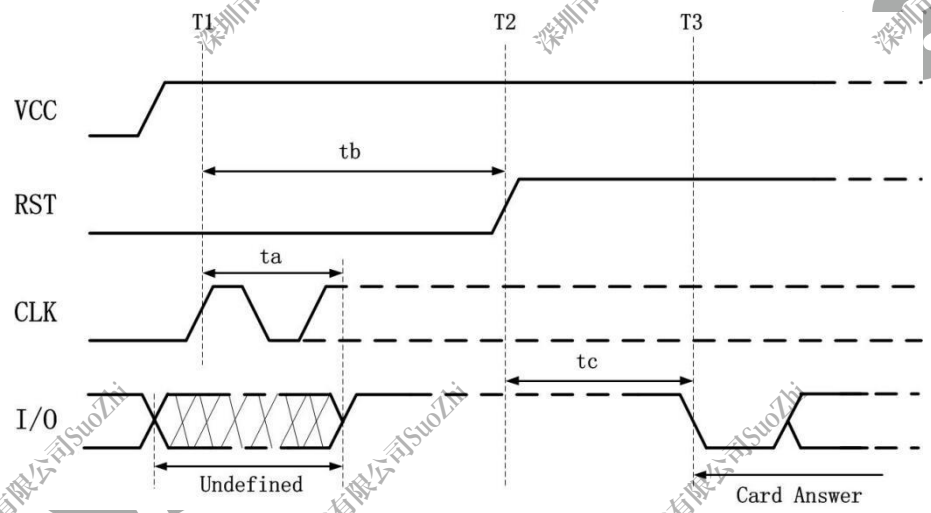


表 6-3 SCR 冷复位时序要求

参数	名称	最小值	典型值	最大值	单位
Reset Hold Time	tb	400	-	-	Tclk
/	ta	-	-	200	Tclk
/	tc	400	-	40000	Tclk

激活结束时(RST处于低电平状态，VCC通电，接口设备中I/O处于接收模式，CLK提供一个合适和稳定的时钟信号)，卡准备好了冷复位。卡在冷复位前内部处于不定态。

如图6-11所示，时钟信号在T1时间作用于CLK。在CLK (T1 + ta)后200个时钟周期(时延ta)，卡应该将I/O设置为高电平时钟信号。冷复位需要在CLK信号保持（T1 + tb）时间之后，将RST保持在低电平状态至少400个时钟周期（延迟tb）。当RST状态为低电平时，接口设备忽略I/O上的状态。

在时间Tb时，RST被置于高电平状态。I/O上的响应应该在RST上(T2 + tc)信号上升沿之后的400到40000时钟周期(延迟)之间开始。如果应答没有在40000钟内开始，接口设备应执行去激活操作。

6.8.2.6 SCR 热复位

图 6- 12 SCR 热复位时序框图

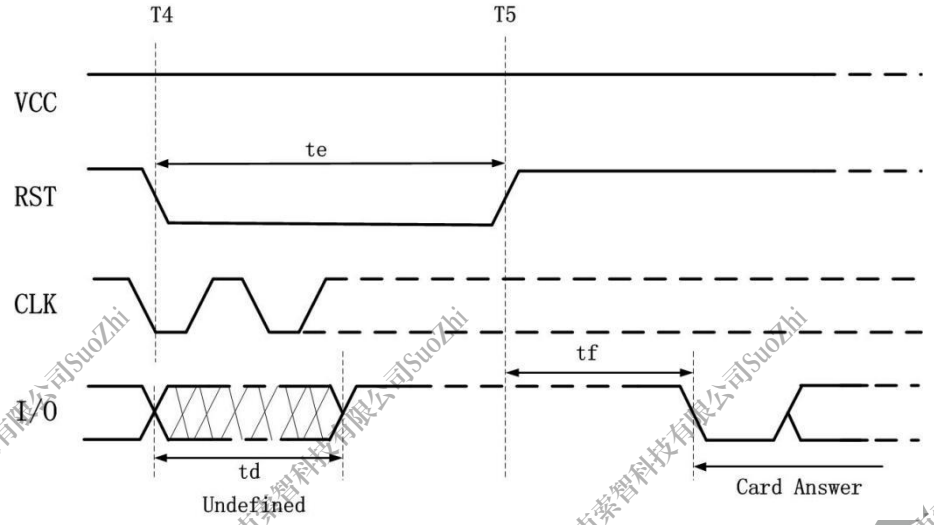


表 6- 4 SCR 热复位时序要求

参数	名称	最小值	典型值	最大值	单位
/	td	-	-	200	Tclk
/	te	400	-	-	Tclk
/	tf	400	-	40000	Tclk

热复位与冷复位不同，接口设备可能会在任意时刻复位卡，即使在回答复位时，也不能在接收前强制复位字符TS和T0。小于4 464 （= 12 × 372）个时钟周期时，不应启动热复位字符T0的前缘之后。

如图6-12所示，当VCC及CLK信号稳定后，接口设备在T4时刻通过将RST设置为低电平（延迟te时间）来发起热复位。将RST保持低电平状态后的200个时钟周期内，卡将I/O设置为高电平状态（延迟td时间）。当RST在低电平状态时，接口设备将忽略I/O上的状态。

在T5时刻， RST被置于高电平状态。I/O上的应答将在RST上升沿保持（T5 + tf）时间后的400到40000时钟周期（延迟）之间开始。如果答案没有在40000钟内开始，接口设备应执行去激活操作。

6.8.3 ISO7816 寄存器列表

模块名	基地址	
SCR	0x40044C00	
寄存器名	**偏移地址**	**描述**
SCR_CSR_REG	0x0000	Smart Card Reader Control and Status Register
SCR_INTEN_REG	0x0004	Smart Card Reader Interrupt Enable Register 1

SCR_INTST_REG	0x0008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR_REG	0x000C	Smart Card Reader FIFO Control and Status Register
SCR_FCNT_REG	0x0010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT_REG	0x0014	Smart Card Reader RX and TX Repeat Register
SCR_DIV_REG	0x0018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM_REG	0x001C	Smart Card Reader Line Time Register
SCR_CTIM_REG	0x0020	Smart Card Reader Character Time Register
SCR_LCTLR_REG	0x0030	Smart Card Reader Line Control Register
SCR_FSM_REG	0x003C	Smart Card Reader FSM Register
SCR_DT_REG	0x0040	Smart Card Reader Debounce Time Register
SCR_FIFO_REG	0x0100	Smart Card Reader RX and TX FIFO Access Point
SCR_VER_REG	0x03FC	Smart Card Reader Version Register

6.8.4 ISO7816 寄存器描述

6.8.4.1 SCR_CSR_REG

偏移地址 : 0x0000			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	R	0x0	SCDET Smart Card Detected This bit is set to ‘1’ when the scdetect input is active at least for a debounce time.
30:25	/	/	/
24	R/W	0x0	SCDETPOL Smart Card Detect Polarity This bit set polarity of scdetect signal. 0: Low Active 1: High Active
23:22	R/W	0x0	Protocol Selection (PTLSEL) 0x0 – T=0. 0x1 – T=1, no character repeating and no guard time is used when T=1 protocol is selected.

			0x2 – Reserved 0x3 – Reserved
21	R/W	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0x0	TSRXE TS Receive Enable When set to ‘1’, the TS character (the first ATR character) will be store in RXFIFO during card session.
19	R/W	0x0	CLKSTPPOL Clock Stop Polarity The value of the scclk output during the clock stop state.
18	R/W	0x0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0x0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0x0	DATAPOL Data Polarity When high, inverse level convention is used (A=’1’, Z=’0’).
15:12	/	/	/
11	R/W	0x0	DEACT Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
10	R/W	0x0	ACT Activation. Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.
9	R/W	0x0	WARMRST Warm Reset Command. Writing ‘1’ to this bit initializes Warm Reset of the Smart Card. This bit is always read as ‘0’.
8	R/W	0x0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in ‘Z’ state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	/

2	R/W	0x0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0x0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0x0	TXEN Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

6.8.4.2 SCR_INTEN_REG

偏移地址 : 0x0004			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt Enable.
22	R/W	0x0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt Enable.
20	R/W	0x0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0x0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0x0	RXDONE RX Done Interrupt Enable.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.

9	R/W	0x0	RXFIFOFULL RX FIFO Full Interrupt Enable.
8:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0x0	TXDONE TX Done Interrupt Enable.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt Enable.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt Enable.

6.8.4.3 SCR_INTST_REG

偏移地址 : 0x0008			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23	R/W1C	0x0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete. Write ‘1’ to clear.
22	R/W1C	0x0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete. Write ‘1’ to clear.
21	R/W1C	0x0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the smart card insertion. Write ‘1’ to clear.
20	R/W1C	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal. Write ‘1’ to clear.
19	R/W1C	0x0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence is successfully completed. Write ‘1’ to clear.
18	R/W1C	0x0	ATRFAIL

			ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails. Write ‘1’ to clear.
17	R/W1C	0x0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards. Write ‘1’ to clear.
16	R/W1C	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: When the smart card clock is stopped. When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the CLKSTOP bit in SCR_CTRL1 register. Write ‘1’ to clear.
15:13	/	/	/
12	R/W1C	0x0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used. Write ‘1’ to clear.
11	R/W1C	0x0	RXDONE RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card. Write ‘1’ to clear.
10	R/W1C	0x0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold. Write ‘1’ to clear.
9	R/W1C	0x0	RXFIFOFULL RX FIFO Full Interrupt. When enabled, this interrupt is asserted if the RX FIFO is filled up. Write ‘1’ to clear.
8:5	/	/	/
4	R/W1C	0x0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used. Write ‘1’ to clear.

3	R/W1C	0x0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the smart card. Write ‘1’ to clear.
2	R/W1C	0x0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold. Write ‘1’ to clear.
1	R/W1C	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out. Write ‘1’ to clear.
0	R/W1C	0x0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO ware transferred to the Smart Card. Write ‘1’ to clear.

6.8.4.4 SCR_FCSR_REG

偏移地址 : 0x000C			**默认值: 0x0000_0100**
位置	**访问**	**默认值**	**描述**
31:11	/	/	/
10	R/W	0x0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed, when ‘1’ is written to this bit.
9	R	0x0	RXFIFOFULL RX FIFO Full.
8	R	0x1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0x0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed, when ‘1’ is written to this bit.
1	R	0x0	TXFIFOFULL TX FIFO Full.
0	R	0x1	TXFIFOEMPTY TX FIFO Empty.

6.8.4.5 SCR_FIFOCNT_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	R/W	0x0	RXFTH RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0x0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.
15:8	R	0x0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0x0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

6.8.4.6 SCR_REPEAT_REG

偏移地址 ：0x0014			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
15:8	/	/	/
7:4	R/W	0x0	RXRPT RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0x0	TXRPT TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

6.8.4.7 SCR_CLKDIV_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	R/W	0x0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used

			to generate the Baud Clock impulses from the system clock. $BAUD = \frac{f_{sysclk}}{2*(BAUDDIV+1)}$
15:0	R/W	0x0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. $f_{scclk} = \frac{f_{sysclk}}{2*(SCCDIV+1)}$ f_{scclk} is the frequency of Smart Card Clock Signal. f_{sysclk} is the frequency of APB Clock.

6.8.4.8 SCR_LTIM_REG

偏移地址 ：0x001C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23:16	R/W	0x0	ATR ATR Start Limit. This 16-bit register defines the maximum time between the rising edge of the scrstn signal and the start of ATR response. ATR Start Limit = 128* ATR* T_{scclk} .
15:8	R/W	0x0	RST Reset Duration. This 16-bit register sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 128* RST* T_{scclk} .
7:0	R/W	0x0	ACT Activation/Deactivation Time. This 16-bit register sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 128* ACT * T_{scclk} . $T_{scclk} = \frac{1}{f_{scclk}}$ is the Smart Card Clock Cycle.

6.8.4.9 SCR_CTIM_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:16	R/W	0x0	CHARLIMIT Character Limit. This 16-bit register sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.
15:8	/	/	/

7:0	R/W	0x0	GUARDTIME Character Guard time. This 8-bit register sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

6.8.4.10 SCR_LCTLR_REG

偏移地址 ：0x0030			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0x0	DSCVPPEN Direct Smart Card Vpp Enable. It provides direct access to SCVPPEN output.
5	R/W	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0x0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0x0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0x0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0x0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0x0	DIRACCPADS Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

6.8.4.11 SCR_FSM_REG

偏移地址 ：0x003C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	R	0x0	ATR_Structure_FSM

23:16	R	0x0	ATR_FSM
15:8	R	0x0	ACT_FSM
7:0	R	0x0	SCR_FSM

6.8.4.12 SCR_DT_REG

偏移地址 ：0x0040			默认值: 0x0000_03FF
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x3ff	SCR_Debounce_Time Set the debounce time value.The time uint is the cycle of SCCLK.

6.8.4.13 SCR_FIFO_REG

偏移地址 ：0x0100			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7:0	R/W	0x0	FIFO_DATA This 8-bit register provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

6.8.4.14 SCR_VER_REG

偏移地址 ：0x03FC			默认值: 0x0001_0000
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
24:16	R	0x1	GEN_VER Generation version.
15:8	R	0x0	SUB_VER Sub version.
7:0	R	0x0	PRJ_VER Project version.

6.9 通用模数转换器(GPADC)

6.9.1 概述

GPADC是一个带有8通道多路复用器的12位采样模拟数字转换器。该ADC是一种逐次逼近寄存器（SAR）转换器。

主要特性如下：

- 12 位分辨率和 10 位有效位的 SAR 型模数转换器

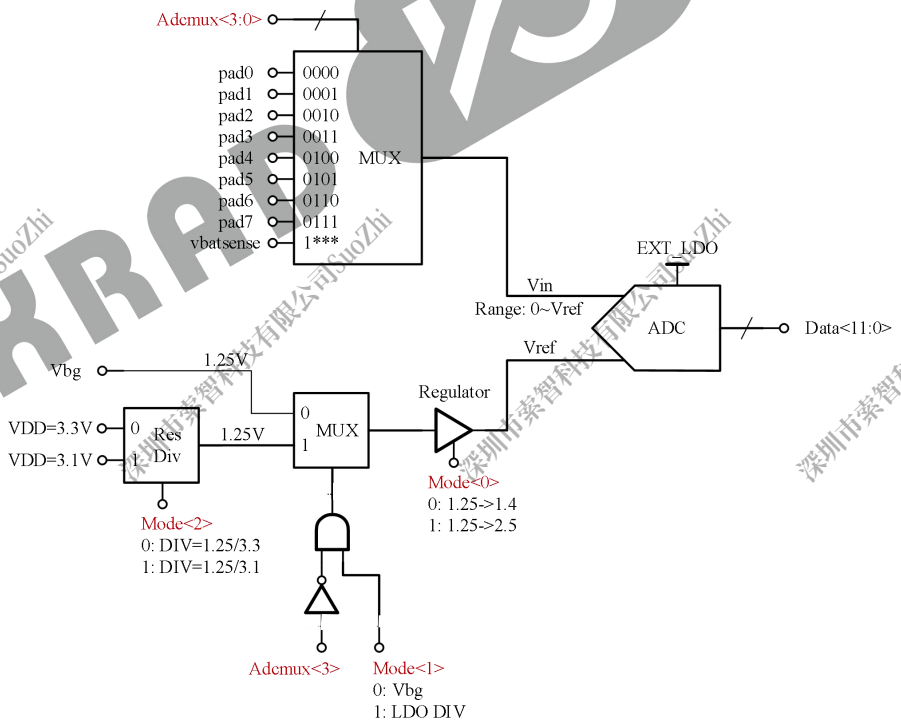
- 8 通道多路复用器，第 9 通道专门用于 VBAT 电压检测
- FIFO 数据寄存器深度为 64
- 电源电压：VDD_EXT （1.8~3.3V），模拟输入范围：0 ~ 2.5V
- 最大采样频率:1MHz
- 支持自校准
- 支持数据比较和中断
- 支持四种操作模式
  - 单次转换模式
  - 单次循环转换模式
  - 连续转换模式
  - 突发转换模式

6.9.2 功能描述

6.9.2.1 模块框图

GPADC逻辑框图如下图所示。

图 6- 13 GPADC 逻辑框图



GPADC的其他特性描述如下。

- 测量 0~7 通道时，Vref 的产生受控于 Mode<2:0>，如下表所示。

Mode<2:0>	Description for Vref Generation
000	Vref=1.4V, regulated from Vbg(1.25V)

001	Vref=2.5V, regulated from Vbg(1.25V)
010	Vref=1.4V, generated from 3.3V VDD
011	Vref=2.5V, generated from 3.3V VDD
100	Same to case 000
101	Same to case 001
110	Vref=1.4V, generated from 3.1V VDD
111	Vref=2.5V, generated from 3.1V VDD

- 测量 8 通道 VBAT 电压时，Vref 的产生仅受控于 Mode<0>，如下表所示。

Mode<0>	**Description for Vref Generation**
0	Vref=1.4V, regulated from Vbg(1.25V)
1	Vref=2.5V, regulated from Vbg(1.25V)

- Worst case 情况下，Vref 源的切换需要 10us 进行建立。
- VBAT sense = 1/3 * VBAT。
- 增加低功耗模式。

6.9.2.2 接口信号

表 6- 5 GPADC 接口信号

信号名称	**描述**	**管脚说明**	**类型**
GPADC0	Analog Input	IO	Analog
GPADC1	Analog Input	IO	Analog
GPADC2	Analog Input	IO	Analog
GPADC3	Analog Input	IO	Analog
GPADC4	Analog Input	IO	Analog
GPADC5	Analog Input	IO	Analog
GPADC6	Analog Input	IO	Analog
GPADC7	Reserved	Reserved	Reserved
GPADC8	VBAT Input	VBAT	Analog

6.9.2.3 工作模式

- 单次转换模式

GPADC 在指定的通道完成一次转换，转换数据更新在对应通道的数据寄存器中。

- 单次循环转换模式

GPADC 在所有指定的通道完成一个周期转换，转换数据更新在对应通道的数据寄存器中。

- 连续转换模式

GPADC 在所有指定的通道连续转换直到软件停止，转换数据更新在对应通道的数据寄存器中。

- 突发转换模式

GPADC 采样和转换在指定通道进行，并将结果顺序地存入 FIFO, FIFO 深度为 32 并支持中断控制。

6.9.3 GPADC 寄存器列表

模块名	基地址	
GPADC	0x40043000	
寄存器名	**偏移地址**	**描述**
GP_SR_CON_REG	0x0000	GPADC Sample Rate Configure Register
GP_CTRL_REG	0x0004	GPADC Control Register
GP_CS_EN_REG	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC_REG	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS_REG	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA_REG	0x0014	GPADC FIFO Data Register
GP_CDATA_REG	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC_REG	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC_REG	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC_REG	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS_REG	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS_REG	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS_REG	0x0038	GPADC Data Interrupt Status Register
GP_CHn_CMP_DATA_REG	0x0040 + 4 * n	GPADC CH n Compare Data Register
GP_CHn_DATA_REG	0x0080 + 4 * n	GPADC CH n Data Register

6.9.4 GPADC 寄存器描述

6.9.4.1 GP_SR_CON_REG

偏移地址 : 0x0000			**默认值: 0x0207_0033**
位置	**访问**	**默认值**	**描述**
31:16	R/W	0x207(50K)	FS_DIV.

			ADC Sample Frequency Divider 采样周期=采样时间+量化时间+空闲 采用时间由 TACQ 配置，量化时间固定为 17 个 HOSC 周期 当 FS_DIV>TACQ+17 时，实际采样率为 HOSC/(FS_DIV+1) 当 FS_DIV≤TACQ+17 时，实际采样率为 HOSC/(TACQ+18) CLK_IN/(n+1) Note: HOSC = 26MHz, n = 0x207; HOSC = 40MHz, n = 0x31F
15:0	R/W	0x33(2uS)	TACQ. ADC acquire time CLK_IN/(n+1) Note: HOSC = 26MHz, n = 0x33; HOSC = 40MHz, n = 0x4F

6.9.4.2 GP_CTRL_REG

偏移地址 ：0x0004			**默认值: 0x0080_0000**
位置	**访问**	**默认值**	**描述**
31:24	R/ W	0x0	ADC_FIRST_DLY. ADC First Convert Delay setting, ADC conversion of each channel is delayed by N samples
23:22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS.(Adjust the bandwidth of the ADC amplifier) ADC OP Bias
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 01: Single-cycle conversion mode 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN. ADC Calibration 1: start Calibration, it is clear to 0 after calibration
16	R/W	0x0	ADC_EN. ADC Function Enable 0: Disable 1: Enable Note: the work mode and the channel number must be set before the ADC_EN bit being set.
15:6	/	/	/
5	R/W	0x0	VBAT_DET_EN 0: disable 1: enable

			Note: the 8th channel is designed for VBAT Voltage Detection and this bit should be set to 1 before enable the CH8
4	R/W	0x0	LP_EN 0: disable 1: enable
3:1	R/W	0x0	VREF_MODE_SEL 000: Vref is 1.4V from BG, choose when vdd is 1.6V~3V 001: Vref is 2.5V from BG, choose when vdd is 3V~3.6V 010: Vref is 2.5V from divider of EXT_LDO, choose when vdd=3.3V 110: Vref is 2.5V from divider of EXT_LDO, choose when vdd=3.1V others: reserved
0	R/W	0x0	ADC_LDO_EN 0: disable 1: enable Note: before enabling the ADC function, you must enable the LDO-ADC firstly.

6.9.4.3 GP_CS_EN_REG

偏移地址 : 0x0008			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
[n+16] (n = 0-8)	R/W	0x0	ADC_CHn_CMP_EN Channel n Compare Enable 0: Disable 1: Enable
15:8	/	/	/
[n] (n = 0-8)	R/W	0x0	ADC_CHn_SELECT. Analog input channel n Select 0: Disable 1: Enable

6.9.4.4 GP_FIFO_INTC_REG

偏移地址 : 0x000C			**默认值: 0x0000_1F00**
位置	**访问**	**默认值**	**描述**
31:19	/	/	/
18	R/W	0x0	FIFO_DATA_DRQ_EN ADC FIFO Data DRQ Enable 0:Disable 1:Enable

17	R/W	0x0	FIFO_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN. ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL. Interrupt and DMA request trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/W1C	0x0	FIFO_FLUSH. ADC FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’
3:0	/	/	/

6.9.4.5 GP_FIFO_INTS_REG

偏移地址 : 0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. ADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails
16	R/W1C	0x0	FIFO_DATA_PENDING. ADC FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails
15:14	/	/	/
13:8	R	0x0	RXA_CNT. ADC FIFO available Sample Word Counter

7:0	/	/	/

6.9.4.6 GP_FIFO_DATA_REG

偏移地址 ：0x0014			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:12	/	/	/
11:0	R/W	0xX	GP_FIFO_DATA GPADC Data in FIFO

6.9.4.7 GP_CDATA_REG

偏移地址 ：0x0018			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
11:0	R/W	0x000	GP_CDATA GPADC Calibration Data

6.9.4.8 GP_DATAL_INTC_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
[n] (n = 0-8)	RW	0	CHn_ LOW_IRQ_EN 0: Disable 1: Enable

6.9.4.9 GP_DATAH_INTC_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
[n] (n = 0-8)	RW	0	CHn_ HIGH_IRQ_EN 0: Disable 1: Enable

6.9.4.10 GP_DATA_INTC_REG

偏移地址 ：0x0028			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/

[n] (n = 0-8)	RW	0	CHn_DATA_IRQ_EN 0: Disable 1: Enable

6.9.4.11 GP_DATAL_INTS_REG

偏移地址 ：0x0030			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
[n] (n = 0-8)	RW	0	CHn_ LOW_PENGDING 1: Channel n Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails

6.9.4.12 GP_DATAH_INTS_REG

偏移地址 ：0x0034			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
[n] (n = 0-8)	RW	0	CHn_ HIGH_PENGDING 1: Channel n Voltage High Available Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails

6.9.4.13 GP_DATA_INTS_REG

偏移地址 ：0x0038			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
[n] (n = 0-8)	RW	0	CHn_DATA_ PENGDING 0: NO Pending IRQ 1: Channel n Data Available Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails

6.9.4.14 GP_CHn_CMP_DATA_REG

偏移地址 ：0x0040 + 4 * n (n = 0-8)			默认值: 0x0BFF_0400
位置	**访问**	**默认值**	**描述**
31:28	/	/	/

27:16	R/W	0xBFF	CHn_CMP_HIG_DATA Channel n Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CHn_CMP_LOW_DATA Channel n Voltage Low Value

6.9.4.15 GP_CHn_DATA_REG

偏移地址 : 0x0080 + 4 * n (n = 0-8)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:12	/	/	/
11:0	R	0x000	GP_CHn_DATA Channel n Data

6.10 通用 I/O(GPIO)

6.10.1 概述

XR806 提供了多达 26 个 GPIO(通用 IO)引脚，所有端口都有备用功能，可以通过配置选择实现在 I/O 引脚上多路复用 GPIO 功能。

XR806 中有两种类型的 GPIO 设计：GPIO 和 AGPIO。每个 GPIO 可以配置以下选项:

- 输入/ 输出/ 浮空(Hi-Z)模式
- 输入模式：上拉或下拉
- 输出模式：主动驱动
- 上拉/下拉控制：上拉和下拉内阻 90KΩ（在 PVT 条件下±30%的变化）
- 具有 5 种触发模式的外部中断 IO：高电平、低电平、上升沿、下降沿、双边沿
- 14 个唤醒 IO 可以设置在 hibernate 状态（只用 RTC 域工作）下通过外部中断唤醒系统
- 所有的 IO 可以设置在 STANDBY 模式（RTC 和 AO 域工作）下通过外部中断唤醒系统

数字 IO AGPIO 功能除上述功能外，还可以作为专用的内控信号用于选择数字和模拟功能，这些 IO 即多路复用的 8 通道 ADC（通道 8 是内部连接测量 VBAT 电压）。

注意

PA23 在芯片上电启动过程中必须为高电平，才能保证整个芯片可以正常上电并运行系统。

6.10.2 GPIO 功能描述

表 6- 6 XR806Bxxx GPIO 复用关系表

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC8	FUNC9
PA00	FEM_CTRL1	AUDIO_PWMP	TWI1_SCL	IR_RX	KEY_Y0	PWM5/ECT5
PA01	FEM_CTRL2	AUDIO_PWMN	TWI1_SDA	FLASH_CS1	KEY_Y1	PWM6/ECT6
PA10/WUPIO0	ADC_CH0	SPI0_MOSI	-	UART1_RX	KEY_Y2	IR_TX
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	KEY_Y3	IR_RX
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	KEY_Y4	TWI0_SCL
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	KEY_Y5	TWI0_SDA
PA14/WUPIO4	ADC_CH4	PWM6/ECT6	I2S_DO	UART2_RX	KEY_Y6	-
PA15/WUPIO5	ADC_CH5	SPI0_CS0	I2S_LRCLK	UART2_CTS	KEY_Y7	TWI1_SCL
PA16/WUPIO6	ADC_CH6	SPI0_CLK	-	UART2_RTS	KEY_X0	TWI1_SDA
PA17/WUPIO7	TWI0_SCL	AUDIO_PWMP	32KOSCO	IR_TX	KEY_X1	-
PA18/WUPIO8	TWI0_SDA	AUDIO_PWMN	FEM_CTRL2	FLASH_CS1	KEY_X2	-
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	KEY_X3	AUDIO_PWMP
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	KEY_X4	AUDIO_PWMN
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	KEY_X5	I2S_DO
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	KEY_X6	I2S_LRCLK
PA23/WUPIO13 /TEST	DCXO_PUP_OUT	IR_RX	FEM_CTRL1	FEM_CTRL2	KEY_X7	I2S_MCLK
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	KEY_Y8	-
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	KEY_Y9	-
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	KEY_Y10	SWD_TMS
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	KEY_Y11	SWD_TCK
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	KEY_Y12	I2S_BCLK
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	KEY_Y13	I2S_DI
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	KEY_Y14	I2S_DO
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	KEY_Y15	I2S_LRCLK
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	KEY_Y0	PWM5/ECT5
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	KEY_Y1	PWM6/ECT6

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC8	FUNC9
PA00	FEM_CTRL1	AUDIO_PWMP	TWI1_SCL	IR_RX	KEY_Y0	PWM5/ECT5
PA01	FEM_CTRL2	AUDIO_PWMN	TWI1_SDA	FLASH_CS1	KEY_Y1	PWM6/ECT6
PA10/WUPIO0	ADC_CH0	SPI0_MOSI	-	UART1_RX	KEY_Y2	IR_TX
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	KEY_Y3	IR_RX
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	KEY_Y4	TWI0_SCL
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	KEY_Y5	TWI0_SDA
PA14/WUPIO4	ADC_CH4	PWM6/ECT6	I2S_DO	UART2_RX	KEY_Y6	-
PA15/WUPIO5	ADC_CH5	SPI0_CS0	I2S_LRCLK	UART2_CTS	KEY_Y7	TWI1_SCL
PA16/WUPIO6	ADC_CH6	SPI0_CLK	-	UART2_RTS	KEY_X0	TWI1_SDA
PA17/WUPIO7	TWI0_SCL	AUDIO_PWMP	32KOSCO	IR_TX	KEY_X1	-
PA18/WUPIO8	TWI0_SDA	AUDIO_PWMN	FEM_CTRL2	FLASH_CS1	KEY_X2	-
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	KEY_X3	AUDIO_PWMP
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	KEY_X4	AUDIO_PWMN
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	KEY_X5	I2S_DO
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	KEY_X6	I2S_LRCLK
PA23/WUPIO13 /TEST	DCXO_PUP_OUT	IR_RX	FEM_CTRL1	FEM_CTRL2	KEY_X7	I2S_MCLK
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	KEY_Y8	-
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	KEY_Y9	-
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	KEY_Y10	SWD_TMS
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	KEY_Y11	SWD_TCK
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	KEY_Y12	I2S_BCLK
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	KEY_Y13	I2S_DI
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	KEY_Y14	I2S_DO
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	KEY_Y15	I2S_LRCLK
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	KEY_Y0	PWM5/ECT5
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	KEY_Y1	PWM6/ECT6

NOTE

1. 支持 1.8V/3.3V/5V IO 电平标准;其他 IO 只支持 1.8V/3.3V 电平标准;

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC8	FUNC9
PA00	FEM_CTRL1	AUDIO_PWMP	TWI1_SCL	IR_RX	KEY_Y0	PWM5/ECT5
PA01	FEM_CTRL2	AUDIO_PWMN	TWI1_SDA	FLASH_CS1	KEY_Y1	PWM6/ECT6
PA10/WUPIO0	ADC_CH0	SPI0_MOSI	-	UART1_RX	KEY_Y2	IR_TX
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	KEY_Y3	IR_RX
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	KEY_Y4	TWI0_SCL
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	KEY_Y5	TWI0_SDA
PA14/WUPIO4	ADC_CH4	PWM6/ECT6	I2S_DO	UART2_RX	KEY_Y6	-
PA15/WUPIO5	ADC_CH5	SPI0_CS0	I2S_LRCLK	UART2_CTS	KEY_Y7	TWI1_SCL
PA16/WUPIO6	ADC_CH6	SPI0_CLK	-	UART2_RTS	KEY_X0	TWI1_SDA
PA17/WUPIO7	TWI0_SCL	AUDIO_PWMP	32KOSCO	IR_TX	KEY_X1	-
PA18/WUPIO8	TWI0_SDA	AUDIO_PWMN	FEM_CTRL2	FLASH_CS1	KEY_X2	-
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	KEY_X3	AUDIO_PWMP
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	KEY_X4	AUDIO_PWMN
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	KEY_X5	I2S_DO
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	KEY_X6	I2S_LRCLK
PA23/WUPIO13 /TEST	DCXO_PUP_OUT	IR_RX	FEM_CTRL1	FEM_CTRL2	KEY_X7	I2S_MCLK
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	KEY_Y8	-
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	KEY_Y9	-
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	KEY_Y10	SWD_TMS
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	KEY_Y11	SWD_TCK
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	KEY_Y12	I2S_BCLK
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	KEY_Y13	I2S_DI
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	KEY_Y14	I2S_DO
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	KEY_Y15	I2S_LRCLK
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	KEY_Y0	PWM5/ECT5
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	KEY_Y1	PWM6/ECT6

2. 其他功能描述可参考《XR806 PIN MUX.pdf》；

表 6- 7 XR806Axxx GPIO 复用关系表

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	EINTA11
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	EINTA12
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	EINTA13
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	EINTA19
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	EINTA20
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	EINTA21
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	EINTA22
PA23/WUPIO13/ TEST	DCXO_PUP_OUT	IR_RX	FEM_CTRL1	FEM_CTRL2	EINTA23
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	EINTB2
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	EINTB3
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	EINTB4
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	EINTB5
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	EINTB6
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	EINTB7
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	EINTB14
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	EINTB15

NOTE

1. 支持 1.8V/3.3V/5V IO 电平标准;其他 IO 只支持 1.8V/3.3V 电平标准;
2. 其他功能描述可参考《XR806 PIN MUX.pdf》；

6.10.3 GPIO 寄存器列表

模块名	基地址	
GPIO Controller	0x40050000	
寄存器名	**偏移地址**	**描述**
Pn_CFG0_REG	n*0x0024 + 0x00	Port n Configure Register 0 (n = 0,1)

Pn_CFG1_REG	n*0x0024 + 0x04	Port n Configure Register 1 (n = 0,1)
Pn_CFG2_REG	n*0x0024 + 0x08	Port n Configure Register 2 (n = 0,1)
Pn_CFG3_REG	n*0x0024 + 0x0C	Port n Configure Register 3 (n = 0,1)
Pn_DATA_REG	n*0x0024 + 0x10	Port n Data Register (n = 0,1)
Pn_DRV0_REG	n*0x0024 + 0x14	Port n Multi-Driving Register 0 (n = 0,1)
Pn_DRV1_REG	n*0x0024 + 0x18	Port n Multi-Driving Register 1 (n = 0,1)
Pn_PULL0_REG	n*0x0024 + 0x1C	Port n Pull Register 0 (n = 0,1)
Pn_PULL1_REG	n*0x0024 + 0x20	Port n Pull Register 1 (n = 0,1)
Pn_EINT_CFG0_REG	0x0200 + n*0x20 + 0x00	PIO External Interrupt Configure Register 0
Pn_EINT_CFG1_REG	0x0200 + n*0x20 + 0x04	PIO External Interrupt Configure Register 1
Pn_EINT_CFG2_REG	0x0200 + n*0x20 + 0x08	PIO External Interrupt Configure Register 2
Pn_EINT_CFG3_REG	0x0200 + n*0x20 + 0x0C	PIO External Interrupt Configure Register 3
Pn_EINT_CTL_REG	0x0200 + n*0x20 + 0x10	PIO External Interrupt Control Register
Pn_EINT_STA_REG	0x0200 + n*0x20 + 0x14	PIO External Interrupt Status Register
Pn_EINT_DBC_REG	0x0200 + n*0x20 + 0x18	PIO External Interrupt Debounce Register

6.10.4 GPIO 寄存器描述

6.10.4.1 Pn_CFG0_REG

偏移地址 :n*0x24 + 0x00 n=0,1			**默认值: 0x0000_0007**
位置	**访问**	**默认值**	**描述**
[4*m+3:4*m] (m = 0~7)	R/W	0x7	GPIO Group n IO m Config

6.10.4.2 Pn_CFG1_REG

偏移地址 :n*0x24 + 0x04 n=0,1			**默认值: 0x0000_0007**
位置	**访问**	**默认值**	**描述**
[4*(m-8)+3:4*(m-8)] (m = 8~15)	R/W	0x7	GPIO Group n IO m Config Note: The function numbers please refer to the Pin Multiplexing. If this IO is not exist, this field is reserved.

6.10.4.3 Pn_CFG2_REG

偏移地址 :n*0x24 + 0x08 n=0,1			默认值: 0x0000_0007
位置	**访问**	**默认值**	**描述**
[4*(m-16)+3:4*(m-16)] (m = 16~23)	R/W	0x7	GPIO Group n IO m Config Note: The function numbers please refer to the Pin Multiplexing. If this IO is not exist, this field is reserved.

6.10.4.4 Pn_CFG3_REG

偏移地址 :n*0x24 + 0x0C n=0,1			默认值: 0x0000_0007
位置	**访问**	**默认值**	**描述**
[4*(m-24)+3:4*(m-24)] (m = 24~31)	R/W	0x7	GPIO Group n IO m Config Note: The function numbers please refer to the Pin Multiplexing. If this IO is not exist, this field is reserved.

6.10.4.5 Pn_DATA_REG

偏移地址 :n*0x24 + 0x10 n=0,1			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	DATA If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

6.10.4.6 Pn_DRV0_REG

偏移地址 :n*0x24 + 0x14 n=0,1			默认值: 0x0000_0001
位置	**访问**	**默认值**	**描述**
[2*m+1:2*m] (m = 15~0)	R/W	0x1	DRV_STRENGTH 00: level 0 01: level 1 10: level 2 11: level 3 Note: This field is only valid when the related IO is exist.

6.10.4.7 Pn_DRV1_REG

偏移地址 :n*0x24 + 0x18 n=0,1			默认值: 0x0000_0001
位置	**访问**	**默认值**	**描述**
[2*(m-16]+1:2*(m-16)] (m = 31~16)	R/W	0x1	DRV_STRENGTH 00: level 0 01: level 1 10: level 2 11: level 3 Note: This field is only valid when the related IO is exist.

6.10.4.8 Pn_PULL0_REG

偏移地址 :n*0x24 + 0x1C n=0,1			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
[2*m+1:2*m] (m = 15~0)	R/W	0x0	PULL 00: NO PULL 01: Pull-Up 10: Pull-Down 11: / Note: This field is only valid when the related IO is exist.

6.10.4.9 Pn_PULL1_REG

偏移地址 :n*0x24 + 0x20 n=0,1			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
[2*(m-16]+1:2*(m-16)] (m = 31~16)	R/W	0x0	PULL 00: NO PULL 01: Pull-Up 10: Pull-Down 11: / Note: This field is only valid when the related IO is exist.

6.10.4.10 Pn_EINT_CFG0_REG

偏移地址 :0x200 + 0x20*n + 0x00			默认值: 0x0000_0007
位置	**访问**	**默认值**	**描述**
[4*m+3:4*m] (m = 0~7)	R/W	0x0	EINT_MODE 0: Positive Edge 1: Negative Edge 2: High Level

			3: Low Level 4: Double Edge others: / Note: This field is only valid when the related IO is exist.

6.10.4.11 Pn_EINT_CFG1_REG

偏移地址 :0x200 + 0x20*n + 0x04			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
[4*(m-8)+3:4*(m-8)] (m = 8~15)	R/W	0x0	EINT_MODE 0: Positive Edge 1: Negative Edge 2: High Level 3: Low Level 4: Double Edge others: / Note: This field is only valid when the related IO is exist.

6.10.4.12 Pn_EINT_CFG2_REG

偏移地址 :0x200 + 0x20*n + 0x08			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
[4*(m-16)+3:4*(m-16)] (m = 16~23)	R/W	0x0	EINT_MODE 0: Positive Edge 1: Negative Edge 2: High Level 3: Low Level 4: Double Edge others: / Note: This field is only valid when the related IO is exist.

6.10.4.13 Pn_EINT_CFG3_REG

偏移地址 :0x200 + 0x20*n + 0x0C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
[4*(m-24)+3:4*(m-24)] (m = 24~31)	R/W	0x0	EINT_MODE 0: Positive Edge

			1: Negative Edge 2: High Level 3: Low Level 4: Double Edge others: / Note: This field is only valid when the related IO is exist.

6.10.4.14 Pn_EINT_CTRL_REG

偏移地址 :0x200 + 0x20*n + 0x0C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
m (m = 31~0)	R/W	0x0	EINT_IRQEN 0: disable 1: enable Note: This field is only valid when the related IO is exist.

6.10.4.15 Pn_EINT_STA_REG

偏移地址 :0x200 + 0x20*n + 0x14			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
[m] (m = 31~0)	R/W	0x0	EINT_IRQST 0: nothing 1: irq pending write 1 to clear Note: This field is only valid when the related IO is exist.

6.10.4.16 Pn_EINT_DBC_REG

偏移地址 :0x200 + 0x20*n + 0x18			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6:4	R/W	0	Debounce Clock Pre-Scale n The selected clock is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SEL 0: LFCLK 1: HFCLK

7 音频接口(Audio)

7.1 数字音频功放驱动器(Audio-PWM)

7.1.1 概述

XR806具有一个数字差分PWM（DPWM）线路输出驱动器，用于驱动外部D类音频放大器。DPWM线路输出驱动器通过上采样和调制PCM输入来差分驱动Audio_PWMP和Audio_PWMN引脚。DPWM线性输出驱动器的输出幅度受控于VDDIO电压。

主要特性如下：

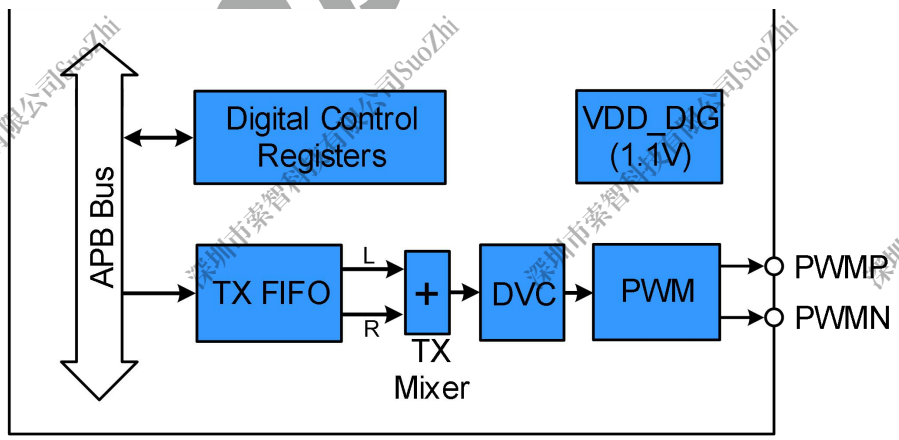
- 单声道数字音频 PWM 线路输出驱动器(CLD)
  - SNR >= 95dB (A-Weighting)
  - THD+N <= -80dB (A-Weighting)
  - 支持8KHz到48KHz的CLD采样率
- 一个 64x18 位 FIFO 用于 CLD 数据传输
- 可编辑的 FIFO 阈值
- 支持 DMA 和中断

7.1.2 功能描述

7.1.2.1 模块框图

Audio-PWM Class-D驱动器逻辑框图如下图所示。

图 7-1 Audio-PWM Class-D 驱动器逻辑框图



7.1.2.2 接口信号

表 7-1 Audio-PWM 接口信号

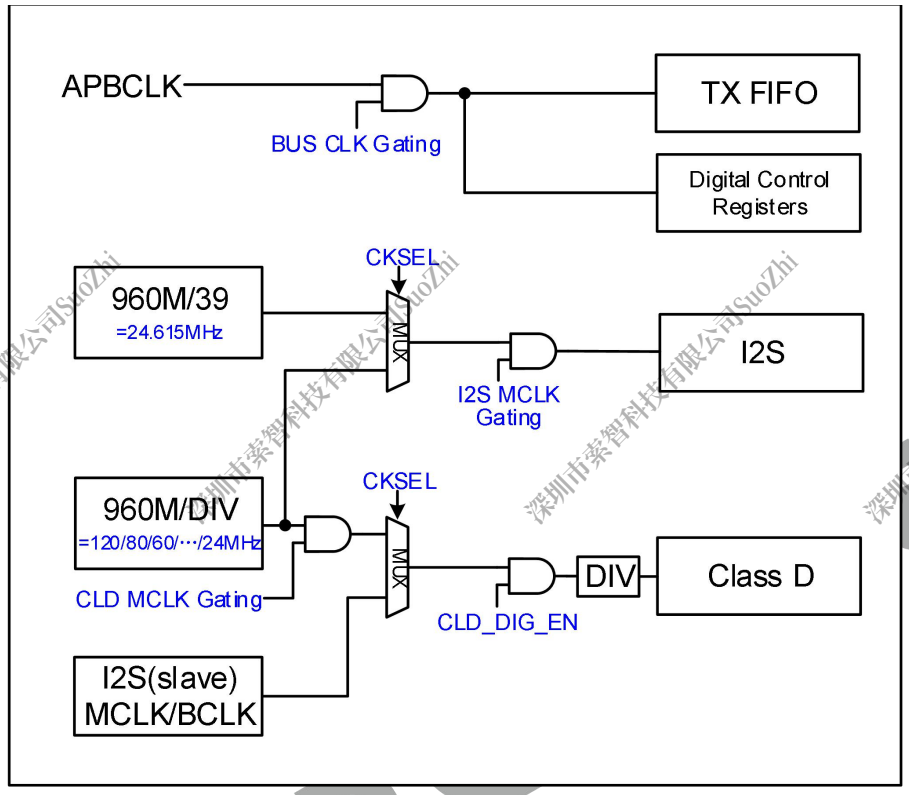
信号名称	类型	描述
PWMP	O	Differential positive output to Digital PWM Class-D.
PWMN	O	Differential negative output to Digital PWM Class-D.

7.1.2.3 时钟复位及中断说明

- 时钟

下图描述了数字音频PWM Class-D驱动器的时钟源。用户可以在时钟控制器单元(CCM)获取时钟设置、配置和门控信息。

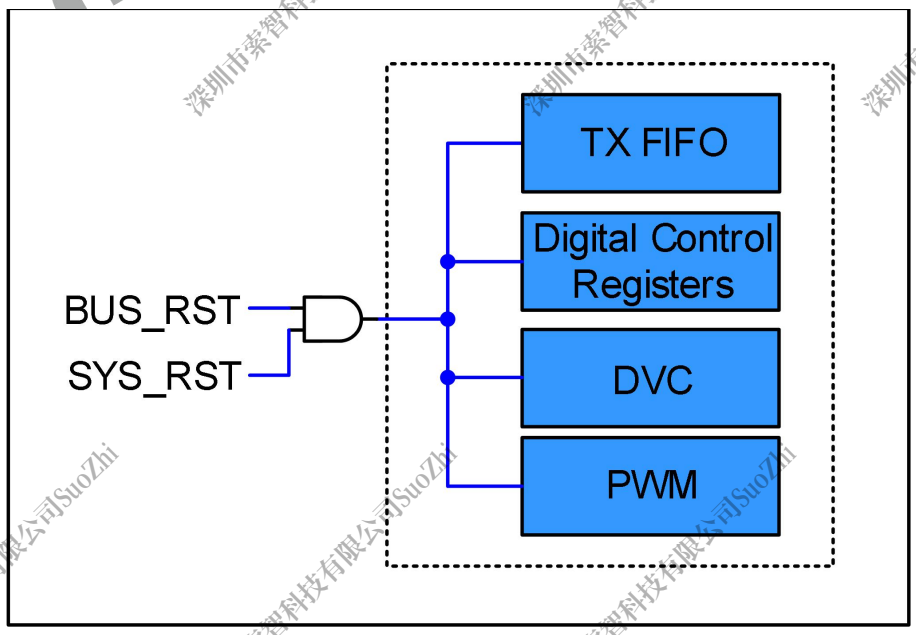
图 7- 2 Audio-PWM Class-D 驱动器时钟系统



- 复位

下图描述了数字音频PWM Class-D驱动器的复位源。SYS_RST和BUS_RST可以复位编解码的数字部分。SYS_RST由系统复位电路提供，BUS_RST产生于CCM模块对应的寄存器。

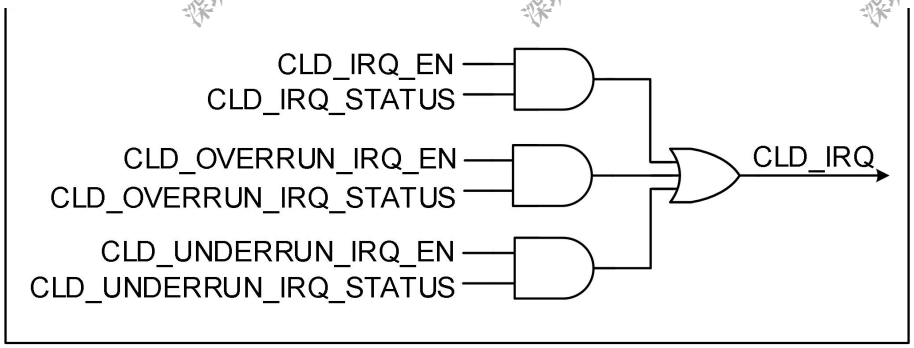
图 7- 3 Audio-PWM Class-D 驱动器复位系统



- 中断

数字音频PWM Class-D驱动器的中断系统如下图所示。

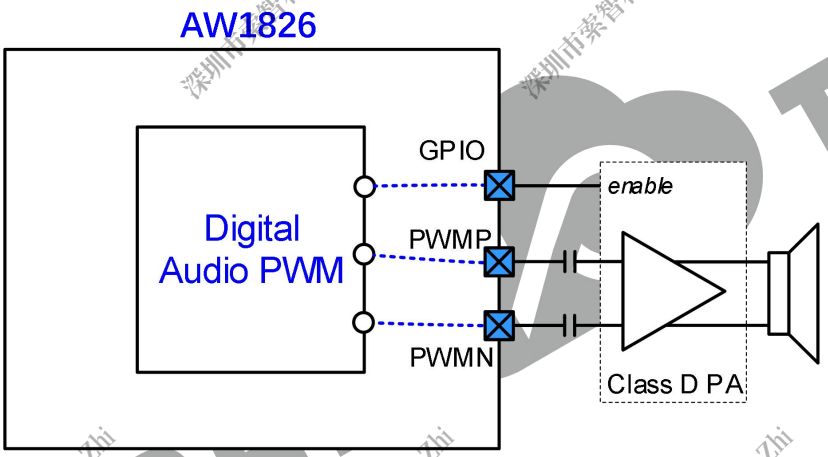
图 7- 4 Audio-PWM Class-D 驱动器中断系统



7.1.2.4 典型应用图示

下图给出了数字音频PWM Class-D驱动器的典型应用框图供参考。

图 7- 5 Audio-PWM Class-D 驱动器应用框图



7.1.3 Audio-PWM Class-D Driver 寄存器列表

模块名	基地址	
Audio PWM Class-D Driver	0x40044000	
寄存器名	**偏移地址**	**描述**
CLD_DIG_CTRL_REG	0x00	Class-D Digital Control Register
CLD_FIFO_CTRL_REG	0x04	Class-D FIFO Control Register
CLD_FIFO_STA_REG	0x08	Class-D FIFO Status Register
CLD_TXDATA_REG	0x0C	Class-D TX DATA Register
CLD_TXCNT_REG	0x10	Class-D TX FIFO Counter Register

7.1.4 Audio-PWM Class-D Driver 寄存器描述

7.1.4.1 CLD_DIG_CTRL_REG

偏移地址 ：0x0000			默认值: 0x0096_CC03
位置	**访问**	**默认值**	**描述**
31	R/W	0x0	Class-D clock enable 0: Disable 1: Enable
30	R/W	0x0	PWM module reset control 0: reset asserted 1: reset de-asserted
29	R/W	0x0	Reserved
28	R/W	0x0	PWM_DIG_EN. PWM Digital Enable 0: Disable 1: Enable
27:26	R/W	0x0	Reserved
25:24	R/W	0x0	PWM MODULATION MODE 00:156x (48k series) 01:136x (44.1k series) 10:128x (Slave Mode) 11:64x (Slave Mode)
23	R/W	0x1	Class-D dither enable 0:disable 1:enable
22:21	R/W	0x0	Class-D dither level selection 00:1 01:3 10:7 11:15
20	R/W	0x1	Class-D mute detection enable 0:disable 1:enable
19:17	R/W	0x3	Class-D mute detection in time: @1/fs 000:16 001:32 010:64 011:128 100:256

			101:512 110:1024 111:2048
16:14	R/W	0x3	clsd_dsm_tun class-d modulating gain control 000:2/8 001:3/8 010:4/8 011:5/8 100:6/8 101:7/8 110: 8/8 111: 9/9
13:12	R/W	0x0	CLD_PTN_SEL CLD Pattern Select 00: Normal(Audio sample from CLD mixer) 01: -6 dB sin wave 10: -60 dB sin wave 11: zero data
11	R/W	0x1	CLD_DVC_ZCD_EN Class-D DVC Zero Cross Detect Enable 0:disable 1:enable
10:4	R/W	0x40	CLD_DVC_VOL (CLD DVC) Class-D DVC volume (-47.25dB To 47.25dB, 0.75dB/Step) 0x00: Mute 0x01: -47.25dB …… 0x3E = -1.5dB 0x3F = -0.75dB 0x40 = 0dB 0x41= 0.75dB 0x42 = 1.5dB …… 0x7F = 47.25dB
3:2	R/W	0x0	Reserved
1:0	R/W	0x3	TX_MIX_CTRL 00: TXL 01: TXR 10: TXL+TXR

			11: (TXL+TXR)/2

7.1.4.2 CLD_FIFO_CTRL_REG

偏移地址 ：0x0004			默认值: 0x0000_1000
位置	**访问**	**默认值**	**描述**
31:27	/	/	/
26	R/W	0x0	SEND_LASAT. Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25	R/W	0X0	reserved
24	R/W	0x0	FIFO_MODE. For18-bits transmitted audio sample: 0: FIFO_I[17:0] = {TXDATA[31:14]} 1: Reserved For 16-bits transmitted audio sample: 0: FIFO_I[17:0] = {TXDATA[15:0], 2'b0} 1: FIFO_I[17:0] = {TXDATA[31:16], 2'b0}
23	/	/	/
22:21	R/W	0x0	CLD_DRQ_CLR_CNT. When TX FIFO available room less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:13	/	/	/
12:7	R/W	0x20	TX_TRIG_LEVEL. TX FIFO Empty Trigger Level (TXTL[5:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ⩽ TXTL Notes: WLEVEL represents the number of valid samples in the TX FIFO Only TXTL[5:0] valid when TXMODE = 0
6	R/W	0x0	CLD_MONO_EN. Class-D Mono Enable 0: Stereo, 32 levels FIFO 1: mono, 64 levels FIFO When enabled, L & R channel send same data

5	R/W	0x0	TX_SAMPLE_BITS. Transmitting Audio Sample Resolution 0: 16 bits 1: 18 bits
4	R/W	0x0	CLD_DRQ_EN. Class-D FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	CLD_IRQ_EN. Class-D FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN. Class-D FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN. Class-D FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH. Class-D FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

7.1.4.3 CLD_FIFO_STA_REG

偏移地址 : 0x0008			**默认值: 0x0080_4008**
位置	**访问**	**默认值**	**描述**
31:24	/	/	/
23	R	0x1	TX_EMPTY. TX FIFO Empty 0: More than one sample point in TX FIFO (>= 1 word) 1: No anyone sample point in TX FIFO
22:15	/	/	/
14:8	R	0x40	TXE_CNT. TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT. TX FIFO Empty Pending Interrupt

			0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/W1C	0x0	TXU_INT. TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT. TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

7.1.4.4 AC_CLD_TXDATA_REG

偏移地址 : 0x000C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	W	0x0	TX_DATA. Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

7.1.4.5 CLD_TXCNT_REG

偏移地址 : 0x0010			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0x0	TX_CNT. TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio Synchronization

7.2 数字音频接口控制器(DAUDIO)

7.2.1 概述

数字音频接口控制器主要用于在系统存储器和编解码芯片之间传输音频数据流。控制器支持标准I2S模式、左对齐模式、右对齐模式、PCM模式和TDM模式。

DAudio的主要特性如下：

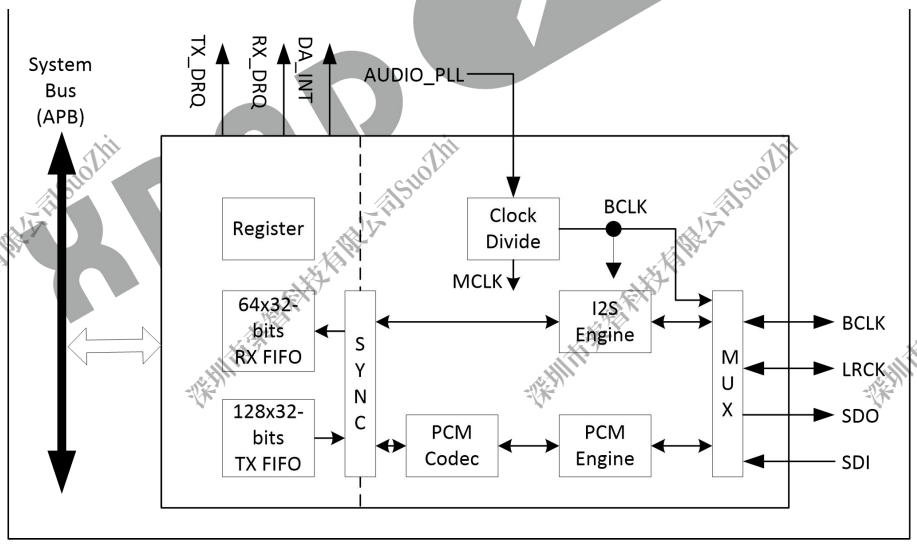
- 符合标准 Philips Inter-IC sound (I2S)总线规范
- 兼容左对齐、右对齐、PCM 模式和时分多路复用(TDM)格式
- 当同时使用 LRCK 和 LRCKR 时，每个接口支持不同的采样周期宽度
- 支持全双工同步工作模式
- 支持主/从模式
- 支持可调接口电压
- 支持 8 位到 32 位的可调音频采样分辨率
- 最多支持 8 个槽位以及 8 位到 32 位的可调宽度
- 支持采样率从 8KHz 到 192KHz
- 支持 1 个数据输出引脚
- 支持 8 位 u-law 和 8 位 A-law 非线性编码
- 一个 32 位宽深度 128 的数据发送 FIFO，一个 32 位宽深度 64 的数据接收 FIFO
- 支持可编程 PCM 帧宽：1 BCLK 宽度(短帧)和 2 BCLKs 宽度(长帧)

7.2.2 功能描述

7.2.2.1 模块框图

DAudio的内部逻辑框图如下图所示。

图 7- 6 DAudio 内部逻辑框图



7.2.2.2 接口信号

下表描述了DAI（DAudio Interface）的外部信号。BCLK和LRCK为双向I/O。当DAI配置为主设备时，BCLK和LRCK为输出引脚;当DAI配置为从设备时，BCLK和LRCK为输入引脚。MCLK是用于外部设备的输出引脚。SDO是串行数据输出脚，SDI是串行数据输入脚。关于通用I/O端口的信息，请参见端口控制器。

表 7- 2 DAudio 接口信号

信号名称	类型	描述
MCLK	O	Digital Audio Interface MCLK Output
LRCK	I/O	Digital Audio Interface Serial Clock
BCLK	I/O	Digital Audio Interface Sample Rate Clock/Sync
SDO	O	Digital Audio Interface Serial Data Output
SDI	I	Digital Audio Interface Serial Data input

7.2.2.3 时钟源

每个DAI控制器有三个不同的时钟。用户可以选择其中一个作为DAI时钟源。下表描述了DAI的时钟源。用户可以看到时钟控制器单元的时钟设置，配置和门控信息。

表 7- 3 DAI 时钟源

时钟名称	描述
Audio_PLL	24.576Mhz or 22.5792Mhz generated by AUDIO-PLL to produce 48KHz or 44.1KHz serial frequency.

7.2.2.4 时序说明

DAI支持标准I2S模式、左对齐I2S模式、右对齐I2S模式、PCM模式和TDM模式。软件可以通过设置DAI控制寄存器来选择DAI工作的其中一个。

图 7- 7 标准 I2S/TDM-I2S 模式时序

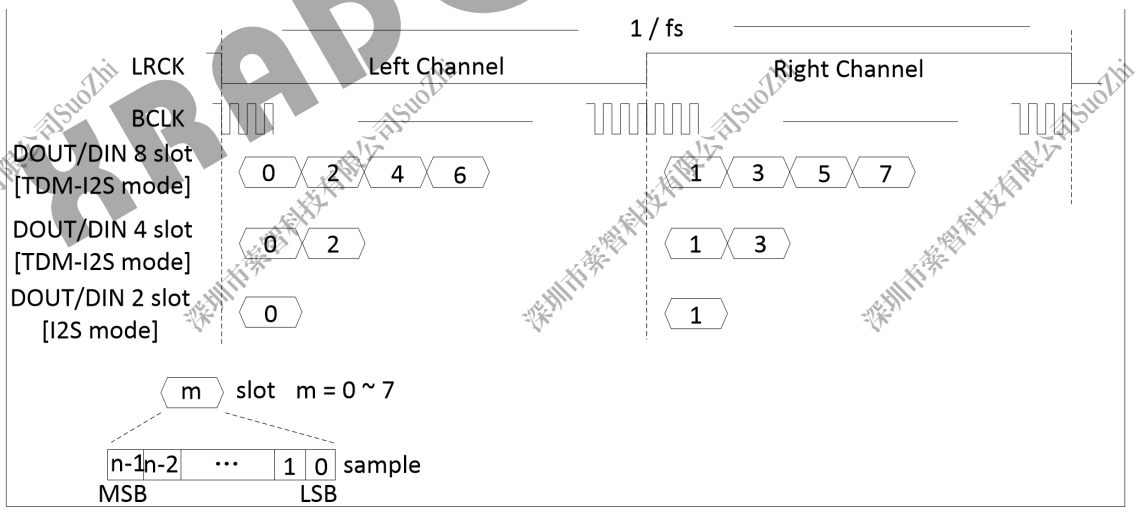


图 7-8 左对齐/TDM-Left 模式时序

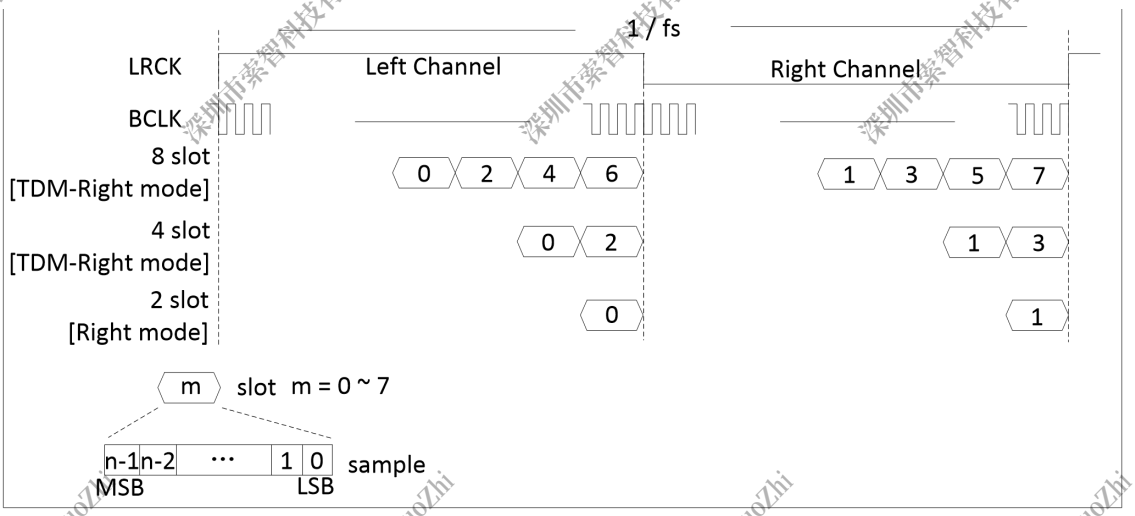
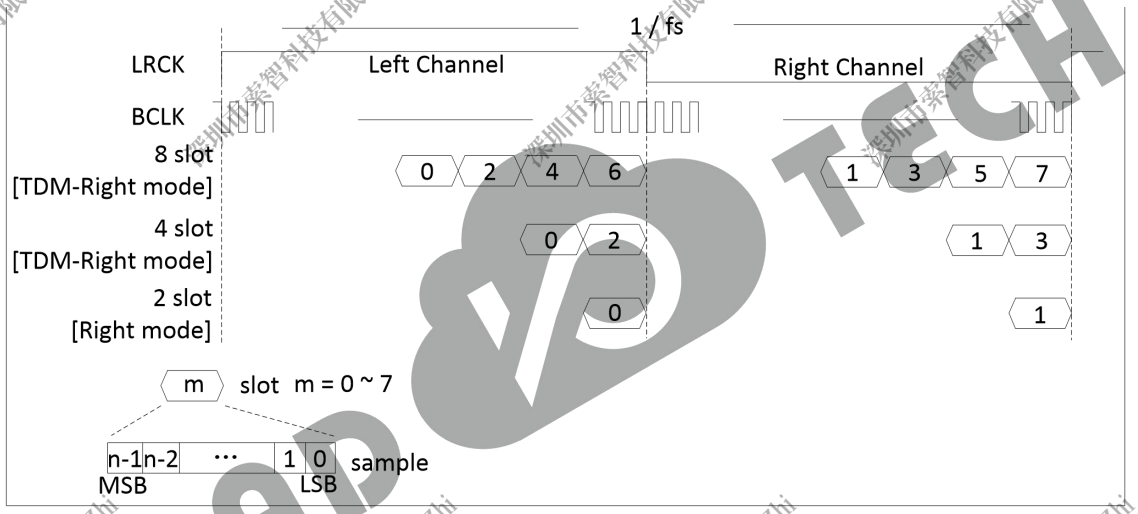


图 7-9 右对齐/TDM-Right 模式时序



7.2.2.5 软件操作

DAI的软件操作分为五个步骤：系统设置、DAI初始化、通道设置、DMA设置和使能/关闭模块。下面几节将详细描述这五种设置。

- 系统设置

系统设置的第一步是正确编程GPIO。因为DAI端口是多路复用引脚，用户可以在引脚复用规范中找到这一功能。DAI的时钟源配置需要遵守以下流程。

首先，必须通过CCMU中的PLL_AUDIO_CTRL_REG的PLL_ENABLE位重置音频锁相环。

第二步，必须在PLL_AUDIO_CTRL_REG中设置音频锁的频率，音频锁相环的配置可查阅时钟源说明。

第三步，当检测到PLL_AUDIO_CTRL_REG的LOCK位变为1时，必须通过DAI0_CLK_REG/DAI1_CLK_REG打开DAI门控。

最后，必须重置DAI的BUS_RST_REG3的位[13:12]，并通过BUS_GATING_REG2的位[13:12]打开DAI总线开关。

- DAI 初始化

系统设置完成后，就可以设置DAI的寄存器了。

首先，必须通过将对应寄存器位写0来关闭全局启用位(DAI_CTL[0])、 TX启用位(DAI_CTL[2])和RX启用位(DAI_CTL[1])。

之后，必须通过将DAI_FCTL[25:24]寄存器位写0来清除TX/RX FIFO。

最后，通过将DAI_TXCNT/DAI_RXCNT寄存器位写0来清除TX/RX FIFO计数器。

以上便完成了DAI的初始化过程。

- 通道与 DMA 设置

在使用和控制DAI之前，必须先配置TWI。通过TWI配置DAI主模式和从模式，相关配置可以参考DAI的协议以及TWI章节寄存器说明。然后，可以设置平移模式、采样精度、槽宽、帧模式和触发电平，相关寄存器可以在规范中找到。

DAI支持三种传输数据方法。最常见的方式是DMA，在这个应用中只需启用DAI的DRQ功能即可。

- 使能/关闭模块

首先，通过配置寄存器位DAI_CTL[2:1]来使能TX/RX。然后，通过将DAI_CTL中的Globe enable位写为1来启用DAI，将Globe Enable写为0来关闭DAI。

7.2.2.6 电气特性

以下对 DAI 主模式、从模式的时序及要求做简要说明。

- DAI 主模式时序要求

图 7-10 DAI 主模式时序图

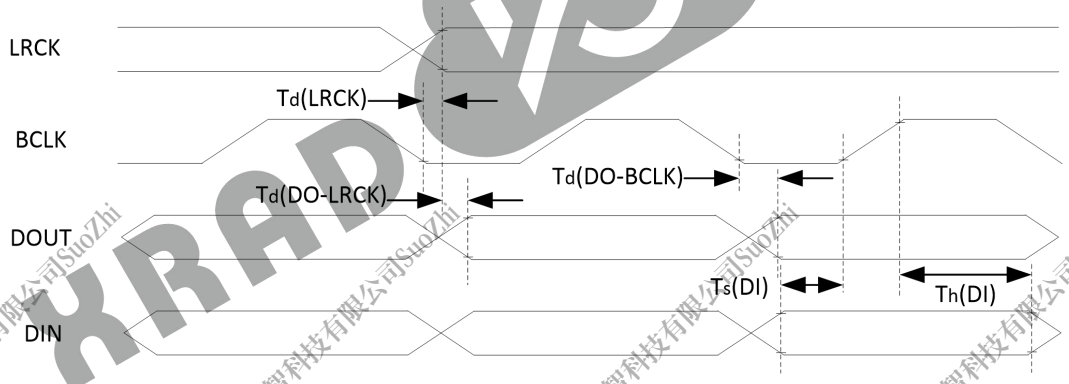


表 7-4 DAI 主模式时序要求

参数	描述	最小值	最大值	单位
Td(LRCK)	LRCK delay	-	10	ns
Td(DO-LRCK)	LRCK to DOUT delay(For LJF)	-	10	ns
Td(DO-BCLK)	BCLK to DOUT delay	-	10	ns
Ts(DI)	DIN setup	4	-	ns
Th(DI)	DIN hold	4	-	ns
Tr	BCLK Rise time	-	8*	ns
Tf	BCLK Fall time	-	8	ns

- DAI 从模式时序要求

图 7- 11 DAI 从模式时序图

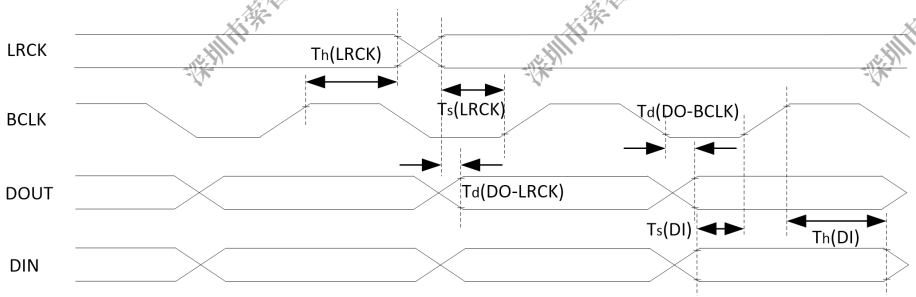


表 7- 5 DAI 主模式时序要求

参数	描述	最小值	最大值	单位
Ts(LRCK)	LRCK setup	4	-	ns
Th(LRCK)	LRCK hold	4	-	ns
Td(DO-LRCK)	LRCK to DOUT delay(For LJF)	-	10	ns
Td(DO-BCLK)	BCLK to DOUT delay	-	10	ns
Ts(DI)	DIN setup	4	-	ns
Th(DI)	DIN hold	4	-	ns
Tr	BCLK Rise time	-	4	ns

7.2.3 DAUDIO 寄存器列表

模块名	基地址	
Digital Audio	0x40042C00	
寄存器名	**偏移地址**	**描述**
DA_CTL	0x0000	Digital Audio Control Register
DA_FMT0	0x0004	Digital Audio Format Register 0
DA_FMT1	0x0008	Digital Audio Format Register 1
DA_ISTA	0x000C	Digital Audio Interrupt Status Register
DA_RXFIFO	0x0010	Digital Audio RX FIFO Register
DA_FCTL	0x0014	Digital Audio FIFO Control Register
DA_FSTA	0x0018	Digital Audio FIFO Status Register
DA_INT	0x001C	Digital Audio DMA & Interrupt Control Register

DA_TXFIFO	0x0020	Digital Audio TX FIFO Register
DA_CLKD	0x0024	Digital Audio Clock Divide Register
DA_TXCNT	0x0028	Digital Audio TX Sample Counter Register
DA_RXCNT	0x002C	Digital Audio RX Sample Counter Register
DA_CHCFG	0x0030	Digital Audio Channel Configuration register
DA_TX0CHCFG	0x0034	Digital Audio TX0 Channel Configuration register
DA_TX1CHSEL	0x0038	Digital Audio TX1 Channel Select Register
DA_TX2CHSEL	0x003C	Digital Audio TX2 Channel Select Register
DA_TX3CHSEL	0x0040	Digital Audio TX3 Channel Select Register
DA_TX0CHMAP	0x0044	Digital Audio TX0 Channel Mapping Register
DA_TX1CHMAP	0x0048	Digital Audio TX1 Channel Mapping Register
DA_TX2CHMAP	0x004C	Digital Audio TX2 Channel Mapping Register
DA_TX3CHMAP	0x0050	Digital Audio TX3 Channel Mapping Register
DA_RXCHSEL	0x0054	Digital Audio RX Channel Select register
DA_RXCHMAP	0x0058	Digital Audio RX Channel Mapping Register

7.2.4 DAUDIO 寄存器描述

7.2.4.1 DA_CTRL_REG

偏移地址 ：0x0000			**默认值: 0x0006_0000**
位置	**访问**	**默认值**	**描述**
31:19	/	/	/
18	R/W	1	BCLK_OUT 0: input 1: output
17	R/W	1	LRCK_OUT 0: input 1: output
16:9	/	/	/
8	R/W	0	SDO0_EN

			0: Disable, Hi-Z state 1: Enable
7	/	/	/
6	R/W	0	OUT Mute 0: normal transfer 1: force DOUT to output 0
5:4	R/W	0	MODE_SEL Mode Selection 0: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 1: Left mode (offset 0: LJ mode; offset 1: I2S mode) 2: Right-Justified mode 3: Reserved
3	R/W	0	LOOP Loop back test 0: Normal mode 1: Loop back test When set ‘1’, connecting the SDO0 with the SDI
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

7.2.4.2 DA_FMT0_REG

偏移地址 : 0x0004			**默认值: 0x0000_0033**
位置	**访问**	**默认值**	**描述**
31	/	/	/
30	R/W	0	LRCK_WIDTH (only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)

29:20	/	/	/
19	R/W	0	LRCK_POLARITY/LRCKR_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK/LRCKR asserted at the negative edge 1: PCM LRCK/LRCKR asserted at the positive edge
18	/	/	/
17:8	R/W	0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width … n = 1023: 1024 BCLKs width
7	R/W	0	BCLK_POLARITY 0: normal mode, negative edge drive and positive edge sample 1: invert mode, positive edge drive and negative edge sample
6:4	R/W	3	SR Sample Resolution 0: Reserved 1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit
3	R/W	0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge BCLK_POLARITY = 1, use positive edge
2:0	R/W	0x3	SW Slot Width Select 0: Reserved

			1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit

7.2.4.3 DA_CTRL_REG

偏移地址 : 0x0008			**默认值: 0x0000_0030**
位置	**访问**	**默认值**	**描述**
31:8	/	/	
7	R/W	0	RX MLS MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0	TX MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	3	SEXT Sign Extend in slot [sample resolution < slot width] 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position 2: Reserved 3: Transfer 0 after each sample in each slot
3:2	R/W	0	RX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law
1:0	R/W	0	TX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law

7.2.4.4 DA_ISTA_REG

偏移地址 ：0x000C			默认值: 0x0000_0010
位置	**访问**	**默认值**	**描述**
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write 1 to clear this interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt when data in TX FIFO are less than TX trigger level Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
3	/	/	/
2	R/W	0	RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write 1 to clear this interrupt
1	R/W	0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt
0	R/W	0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ when data in RX FIFO are more than RX trigger level Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.

7.2.4.5 DA_RXFIFO_REG

偏移地址 ：0x0010			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	R	0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

7.2.4.6 DA_FCTL_REG

偏移地址 ：0x0014			默认值: 0x0004_00F0
位置	**访问**	**默认值**	**描述**
31	R/W	0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/W	0	FTX Write ‘1’ to flush TX FIFO, self clear to ‘0’.
24	R/W	0	FRX Write ‘1’ to flush RX FIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0	TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[31:0] = {APB_WDATA[31:12], 12’h0}

			Mode 1: FIFO_I[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: APB_RDATA[31:0] = {FIFO_O[31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{FIFO_O[31]}, FIFO_O[31:12]} Mode 2: APB_RDATA [31:0] = {FIFO_O[31:16], 16'h0} Mode 3: APB_RDATA [31:0] = {16{FIFO_O[31], FIFO_O[31:16]}

7.2.4.7 DA_FSTA_REG

偏移地址 : 0x0018			**默认值: 0x1080_0000**
位置	**访问**	**默认值**	**描述**
31:29	/	/	/
28	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0	RXA_CNT RX FIFO Available Sample Word Counter

7.2.4.8 DA_INT_REG

偏移地址 ：0x001C			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:8	/	/	/
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to ‘1’, an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to ‘1’, RXFIFO DMA Request line is asserted if Data is available in RX FIFO.
2	R/W	0	RXUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable

			1: Enable

7.2.4.9 DA_TXFIFO_REG

偏移地址 ：0x0020			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:0	W	0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

7.2.4.10 DA_CLKD_REG

偏移地址 ：0x0024			默认值: 0x0000_0000
位置	**访问**	**默认值**	**描述**
31:9	/	/	/
8	R/W	0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.
7:4	R/W	0	BCLKDIV BCLK Divide Ratio from PLL2 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192
3:0	R/W	0	MCLKDIV MCLK Divide Ratio from PLL2 Output 0: reserved

			1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192

7.2.4.11 DA_TXCNT_REG

偏移地址 : 0x0028			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

7.2.4.12 DA_RXCNT_REG

偏移地址 : 0x002C			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:0	R/W	0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

7.2.4.13 DA_CHCFG_REG

偏移地址 : 0x0030			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:10	/	/	/

9	R/W	0	TX_SLOT_HIZ 0: normal mode for the last half cycle of BCLK in the slot 1: turn to hi-z state for the last half cycle of BCLK in the slot
8	R/W	0	TXn_STATE 0: transfer level 0 when not transferring slot 1: turn to hi-z state (TDM) when not transferring slot
7	/	/	/
6:4	R/W	0	RX_SLOT_NUM RX Channel/Slot Number which between CPU/DMA and FIFO 0: 1 channel or slot ... 7: 8 channels or slots
3	/	/	/
2:0	R/W	0	TX_SLOT_NUM TX Channel/Slot Number which between CPU/DMA and FIFO 0: 1 channel or slot ... 7: 8 channels or slots

7.2.4.14 DA_TXnCHSEL_REG

偏移地址 : 0x34 + N*4 (N = 0, 1, 2, 3)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:13	/	/	/
12	R/W	0	TXn_OFFSET TXn offset tune, TXn data offset to LRCK 0: no offset 1: data is offset by 1 BCLKs to LRCK
11:4	R/W	0	TXn_CHEN TXn Channel (slot) enable, bit[11:4] refer to slot [7:0]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable
3	/	/	/
2:0	R/W	0	TXn_CHSEL TXn Channel (slot) number Select for each output 0: 1 channel / slot …

			7: 8 channels / slots

7.2.4.15 DA_TXnCHMAP_REG

偏移地址 ： 0x44 + n*4 (n = 0, 1, 2, 3)			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	/	/	/
30:28	R/W	0	TXn_CH7_MAP TXn Channel7 Mapping 0: 1st sample … 7: 8th sample
27	/	/	/
26:24	R/W	0	TXn_CH6_MAP TXn Channel6 Mapping 0: 1st sample … 7: 8th sample
23	/	/	/
22:20	R/W	0	TXn_CH5_MAP TXn Channel5 Mapping 0: 1st sample … 7: 8th sample
19	/	/	/
18:16	R/W	0	TXn_CH4_MAP TXn Channel4 Mapping 0: 1st sample … 7: 8th sample
15	/	/	/
14:12	R/W	0	TXn_CH3_MAP TXn Channel3 Mapping 0: 1st sample … 7: 8th sample
11	/	/	/

10:8	R/W	0	TXn_CH2_MAP TXn Channel2 Mapping 0: 1st sample … 7: 8th sample
7	/	/	/
6:4	R/W	0	TXn_CH1_MAP TXn Channel1 Mapping 0: 1st sample … 7: 8th sample
3	/	/	/
2:0	R/W	0	TXn_CH0_MAP TXn Channel0 Mapping 0: 1st sample … 7: 8th sample

7.2.4.16 DA_RXCHSEL_REG

偏移地址 : 0x0054			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31:13	/	/	/
12	R/W	0	RX_OFFSET RX offset tune, RX data offset to LRCK 0: no offset 1: data is offset by 1 BCLKs to LRCK
11:3	/	/	
2:0	R/W	0	RX_CHSEL RX Channel (slot) number Select for input 0: 1 channel / slot … 7: 8 channels / slots

7.2.4.17 DA_RXCHMAP_REG

偏移地址 : 0x0058			**默认值: 0x0000_0000**
位置	**访问**	**默认值**	**描述**
31	/	/	/

30:28	R/W	0	RX_CH7_MAP RX Channel7 Mapping 0: 1st sample … 7: 8th sample
27	/	/	/
26:24	R/W	0	RX_CH6_MAP RX Channel6 Mapping 0: 1st sample … 7: 8th sample
23	/	/	/
22:20	R/W	0	RX_CH5_MAP RX Channel5 Mapping 0: 1st sample … 7: 8th sample
19	/	/	/
18:16	R/W	0	RX_CH4_MAP RX Channel4 Mapping 0: 1st sample … 7: 8th sample
15	/	/	/
14:12	R/W	0	RX_CH3_MAP RX Channel3 Mapping 0: 1st sample … 7: 8th sample
11	/	/	/
10:8	R/W	0	RX_CH2_MAP RX Channel2 Mapping 0: 1st sample … 7: 8th sample
7	/	/	/
6:4	R/W	0	RX_CH1_MAP

			TX Channel1 Mapping 0: 1st sample … 7: 8th sample
3	/	/	/
2:0	R/W	0	RX_CH0_MAP RX Channel0 Mapping 0: 1st sample … 7: 8th sample

8 常见问题说明

无。

附录 A： 术语表

表 A-1 术语表

A		
AES	Advanced Encryption Standard	高级加密标注
AGC	Automatic Gain Control	自动增益控制
AHB	AMBA High-speed Bus	先进高性能总线
APB	Advanced Peripheral Bus	高级外设总线
C		
CIR	Consumer IR	用户红外辐射接口
CRC	Cyclic Redundancy Check	循环冗余校验
CSI	CMOS Sensor Interface	CMOS 传感器接口
D		
DES	Data Encryption Standard	数据加密标准
DLL	Delay-Locked Loop	延迟锁相环
DVFS	Dynamic Voltage and Frequency Scaling	动态调频调压
E		
eMMC	Embedded Multi-Media Card	嵌入式多媒体卡
I		
I2S	IIS	集成电路内置音频总线
L		
LSB	Least Significant Bit	最低有效位
M		
MAC	Media Access Control	介质访问控制层
MSB	Most Significant Bit	最高有效位
P		
PCM	Pulse Code Modulation	脉冲编码调制
Q		
SPI	Synchronous Peripheral Interface	串行外设接口
W		
WLAN	Wireless Local Area Network	无线局域网

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